Modifications to the Beetle 1.3

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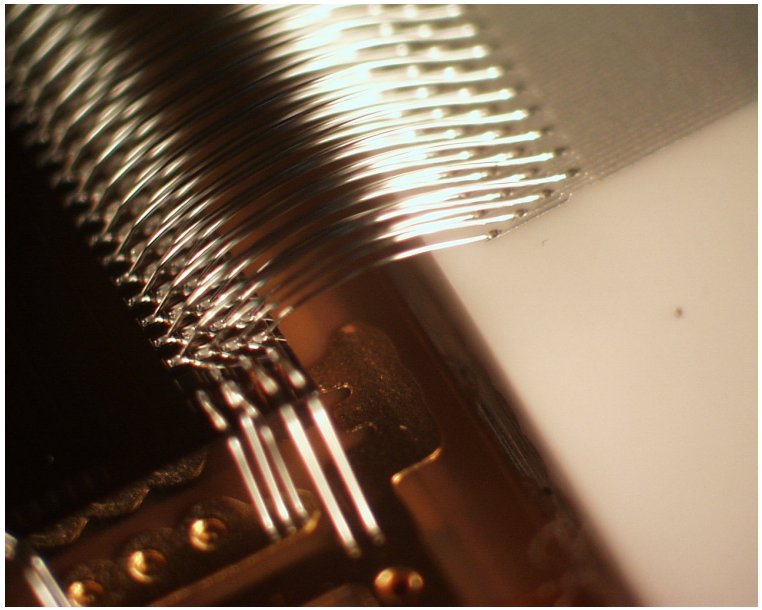
Outline

- Fix of PCN Parity bit
- Beetle Id. number
- Channel crosstalk
  - remove of even/odd crosstalk
  - pipeline modifications
- Further steps



Beetle 1.3
128 staggered input bondings

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Fix of PCN Parity bit

1 port mode

AO[0]	I0	I1	I2	I3	I4	I5	I6	I7	P7	P6	P5	P4	P3	P2	P1	P0

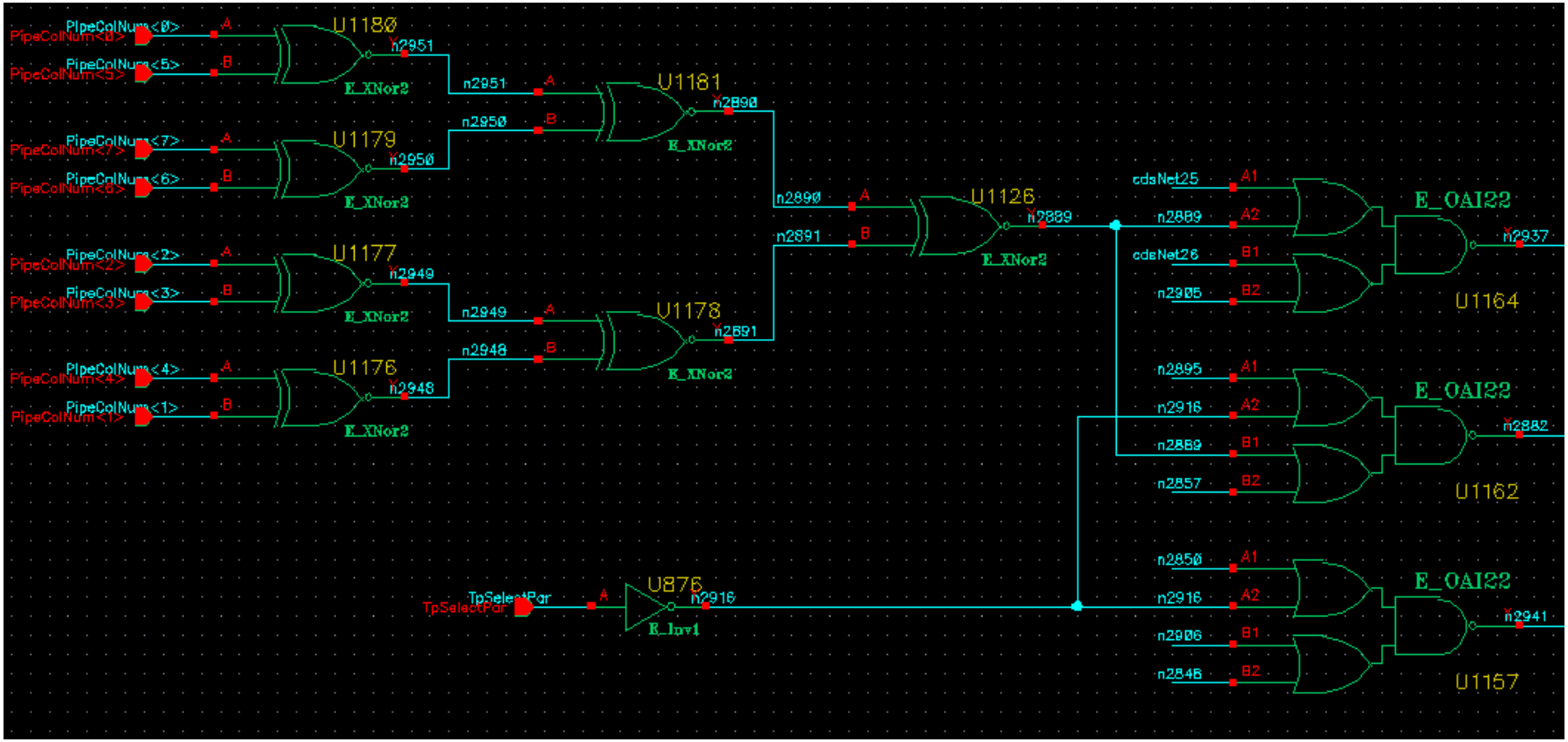
4 port mode

AO[0]	I0	I4	P1	P0
AO[1]	I1	I5	P3	P2
AO[2]	I2	I6	P5	P4
AO[3]	I3	I7	P7	P6

I0	leading bit (always 0)
I1	parity of PCN (even)
I2	Active EDC
I3	parity of reg. CompChTh
I4	parity of reg. CompMask
I5	parity of reg. TpSelect
I6	SEU counter <1>
I7	SEU counter <0>

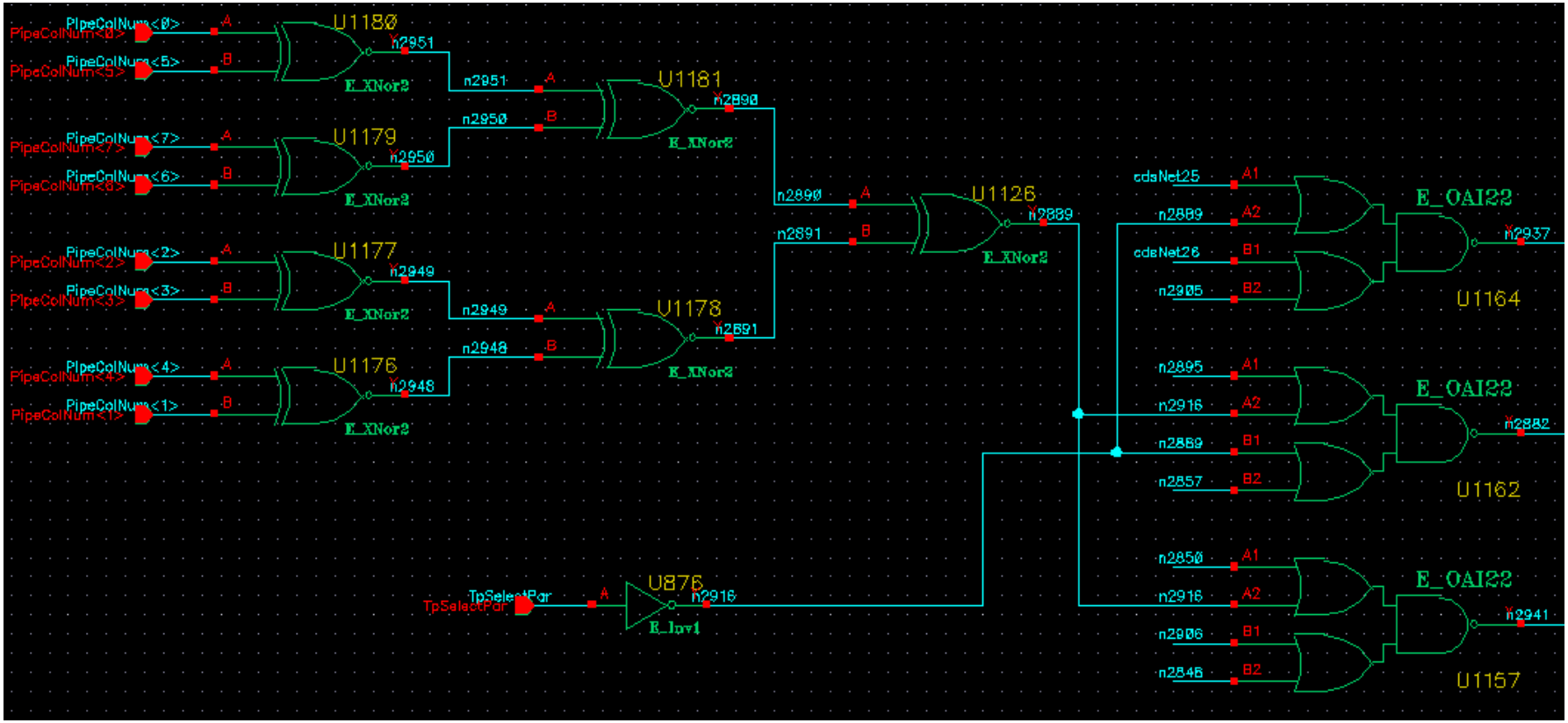
- **Swap position I1 with I5**
- **Same modification as done via FIB patch**
  - **No place and route of control logic**
  - **Manual modification in Cadence**
    Last Metal change
- **LVS check: OK**

PCN - old schematic



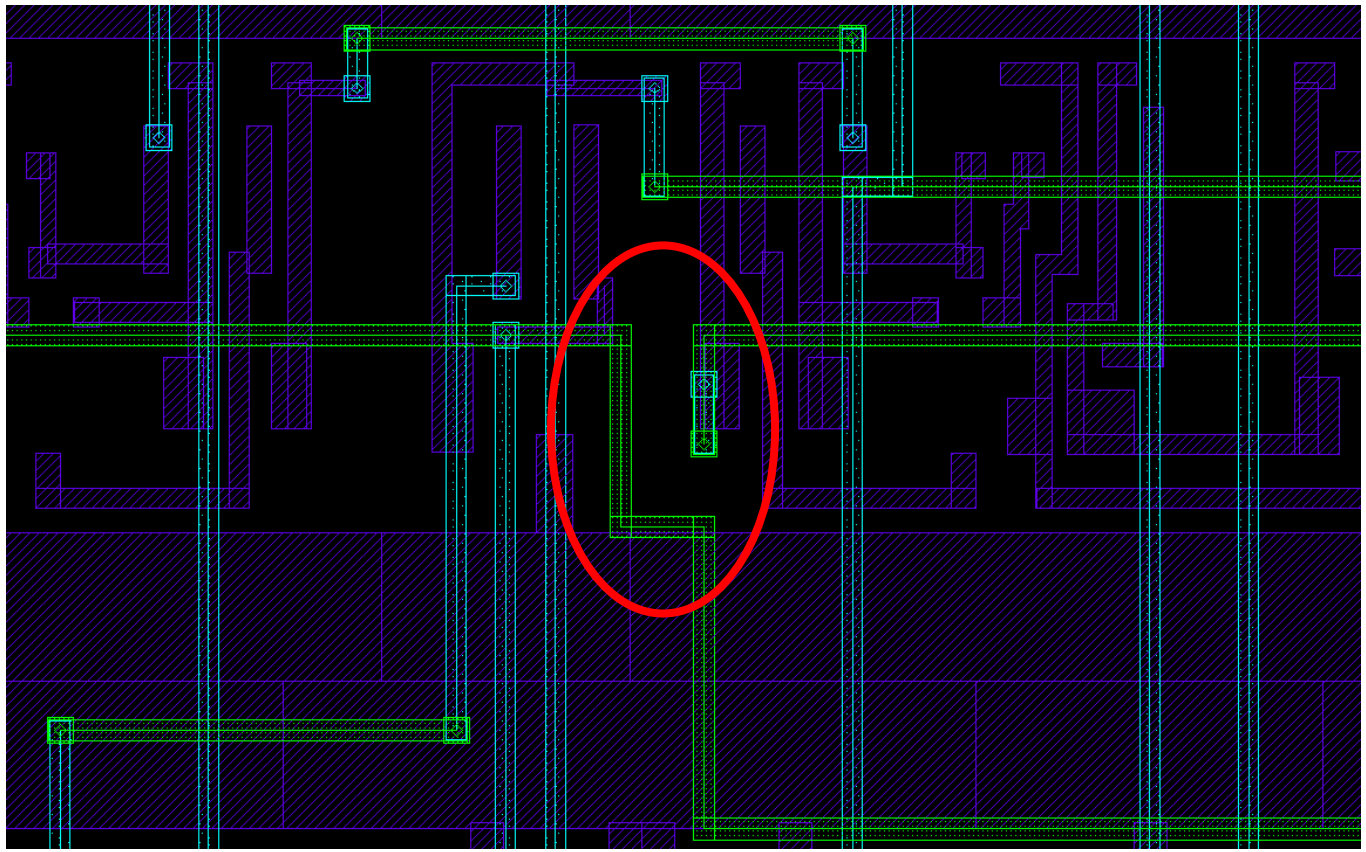
schematic of parity-bit generation (part of MuxScheduler)

PCN - new schematic



new schematic of parity-bit patch

PCN - layout modification



fast control modification: only Last Metal (green) has changed

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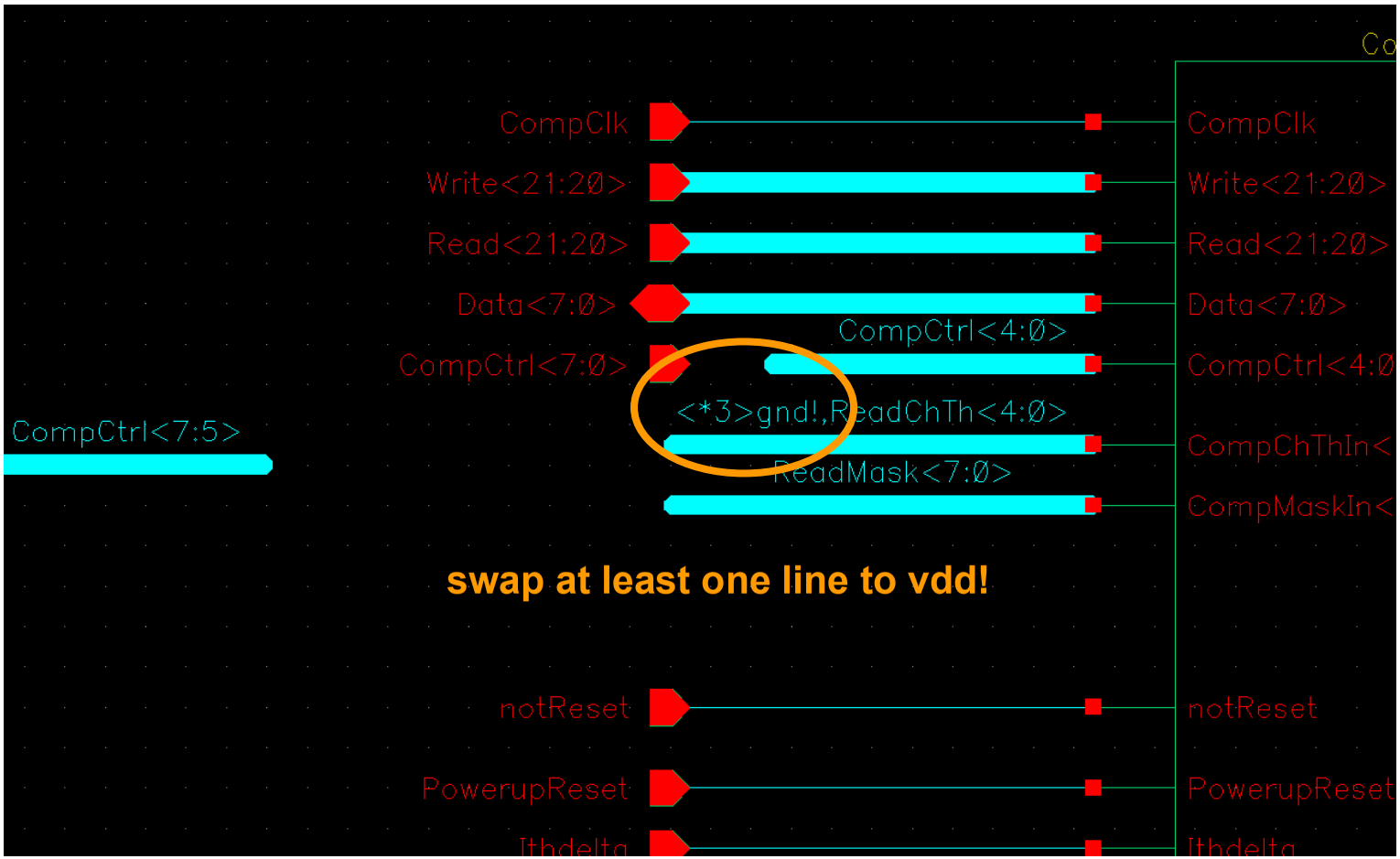
Beetle Id. number

It is impossible to find out the version number of a Beetle chip, because there is no Id. register defined. (except with a microscope)

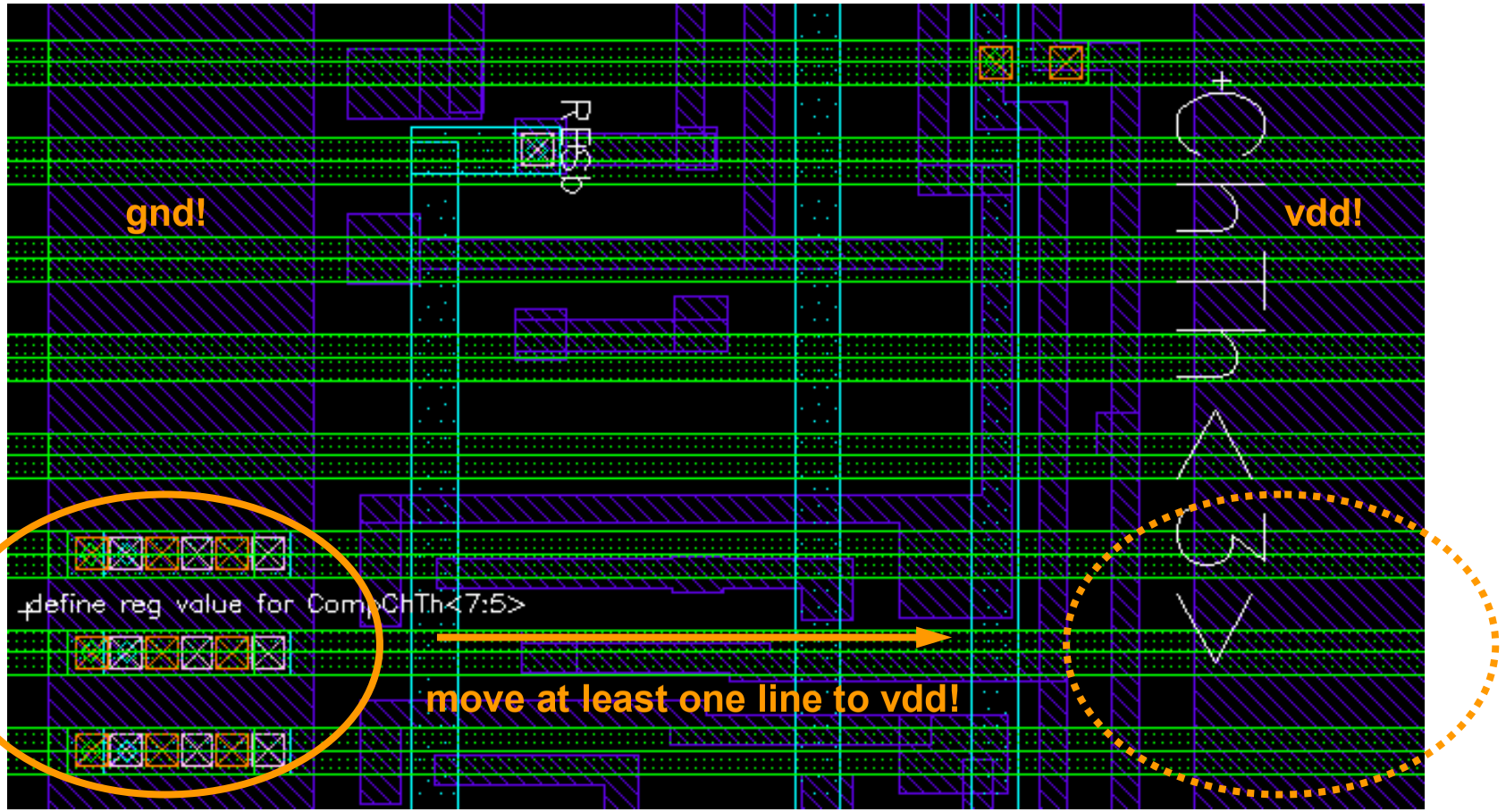
Quick solution:

- **Comparator Channel Threshold register (CompChTh)**
  - **bit 5 to 7 is not used by the comparator**
  - **access via I²C interface to CompChTh<7:5> gives always "1" therefore it is possible to use those bits as a kind of Id. number**
- **Modify one of the bits that a read access gives a "0"**
  - **unique number for 1.4**
- **Easy to change**
- **NO risk of a failure**

Beetle Id. number - schematic



Beetle Id. number - layout



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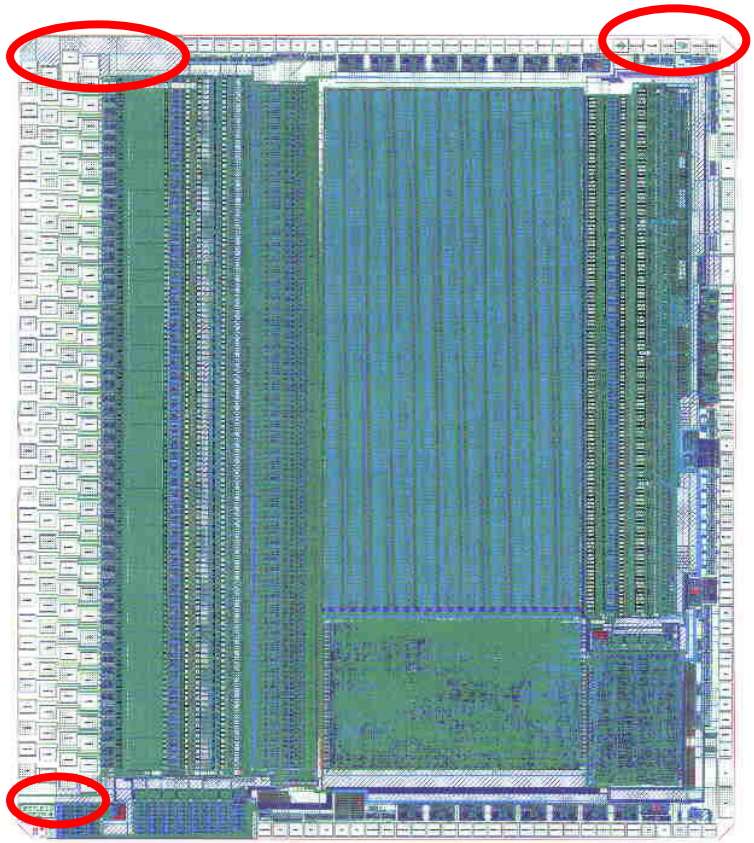
"Visual" modification

Modification of one or two corners of the Beetle (e.g. pad-opening):

- **Easy check of different version numbers** (logo is covered with Polyimide, so it is not so easy to read the version number)
- **Improve the auto-alignment of a automatic bonding machine** (reflective structure)



Beetle 1.3 layout

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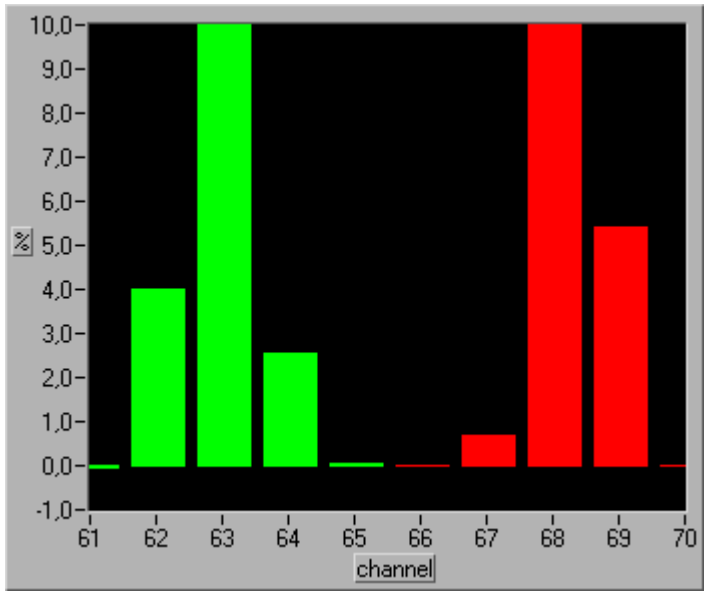
Channel Crosstalk



Testpulse (63. & 68) is standardised to 100%

Channel crosstalk

- **measured a even/odd dependency**

Clarification of crosstalk:

typical Testpulse for a odd channel (e.g. 63):
crosstalk into predecessor channel is larger than into successor channel

typical Testpulse for a even channel (e.g. 68):
crosstalk into successor channel is larger than into predecessor channel

Crosstalk - schematic

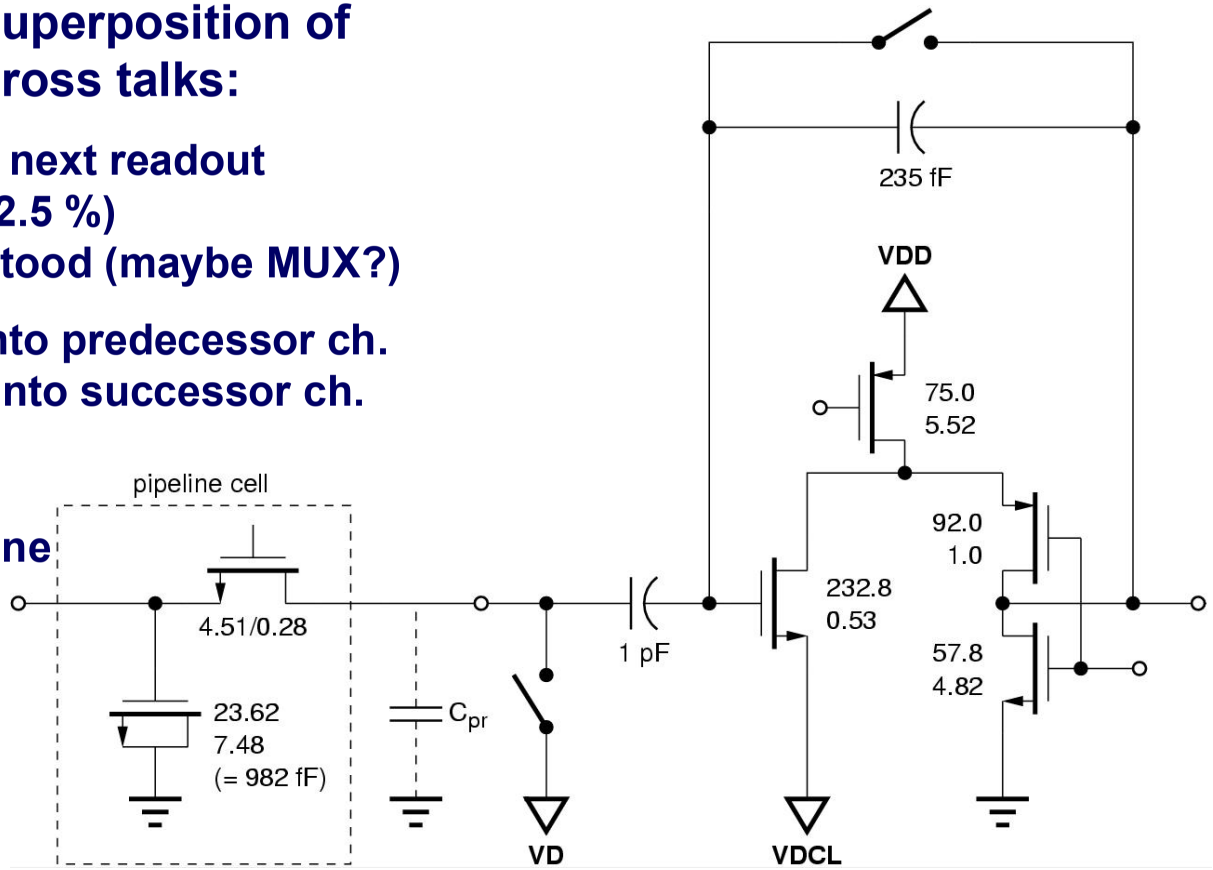
Channel crosstalk is a superposition of at least two different cross talks:

- **general "remainder" into next readout channel (order of 2 % to 2.5 %)**
  ➔ reason yet not understood (maybe MUX?)
- **odd channel: crosstalk into predecessor ch. even channel: crosstalk into successor ch. (order of 2.5 %)**

➔ readout line from Pipeline into Pipeamp

➔ capacitance between adjacent lines ~ 90fF

- **verified in simulation**
- **easy to fix**



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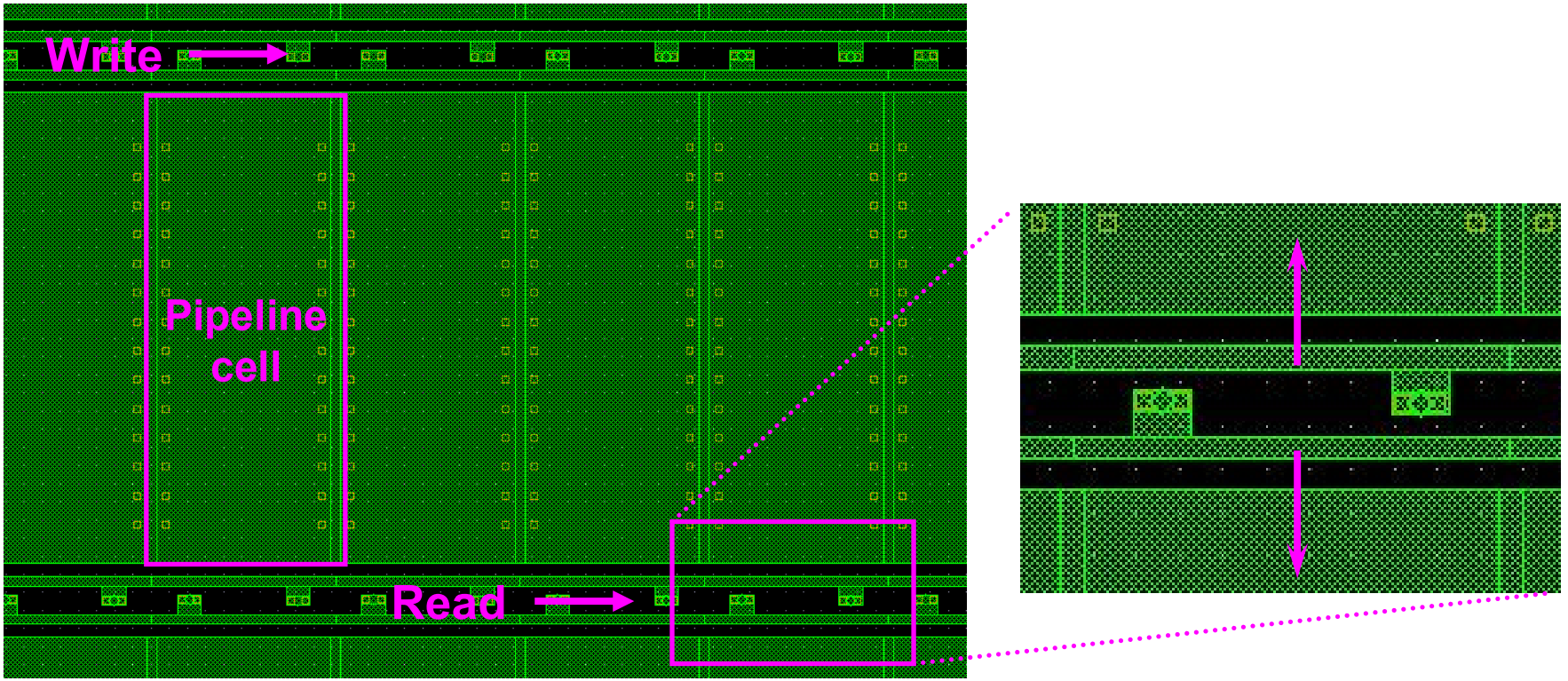
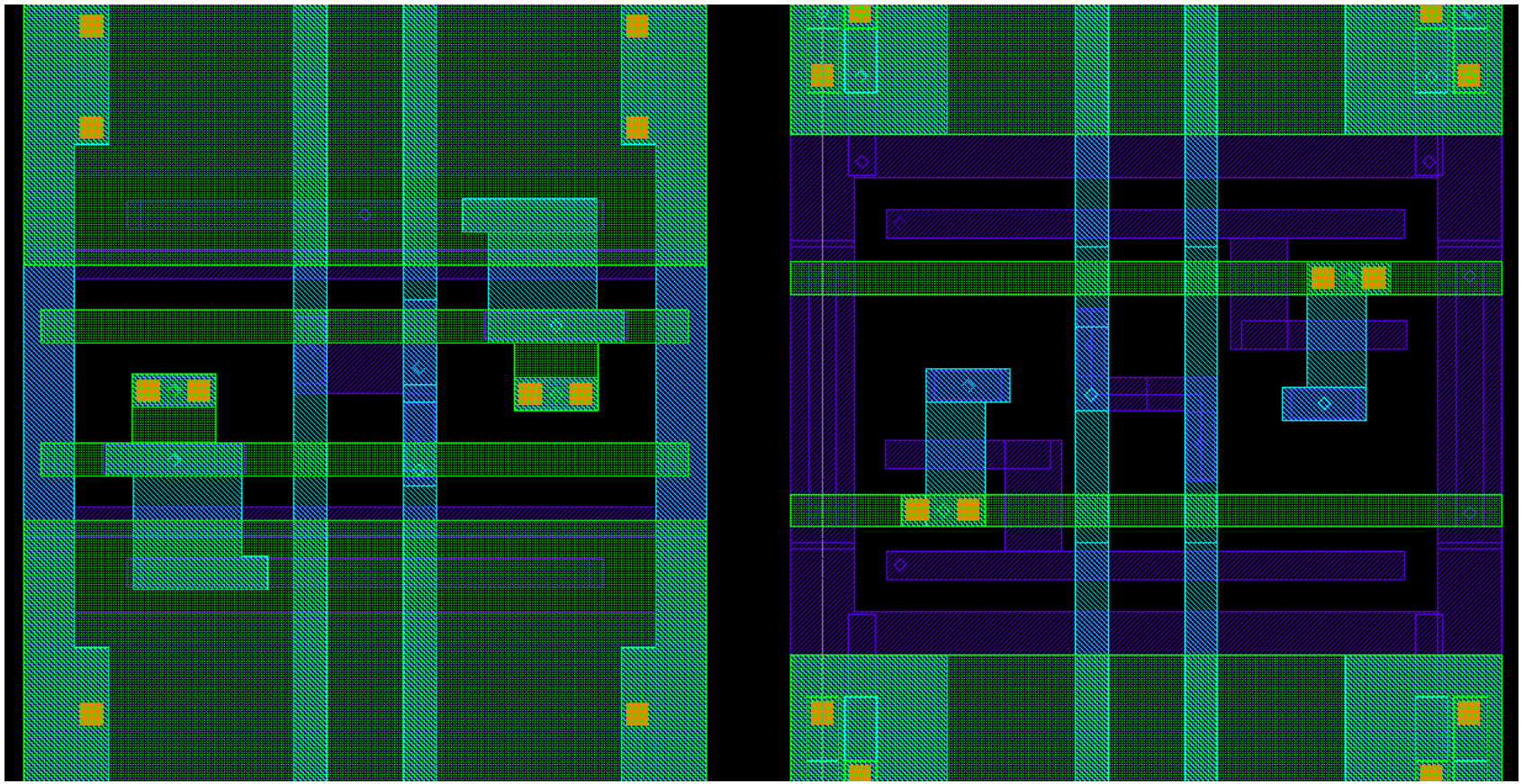
Concept of modification



Pipeline length: ~ 2 mm

Crosstalk - layout modification



old layout

new layout

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New pipeline cell

Calculation and simulation of new pipeline-cell:

- reduced capacitance C_{pr} of Pipeline Readout line from ~300 fF to nearly 100 fF per line
- reduced couple capacitance between to adjacent readout lines from ~90 fF to ~15 fF
- suppress the pipeline crosstalk between two channels to less than 0.3%
- overall readout gain increased by nearly 8%

to be discussed:

- N-well under pipeline-cell
  - characteristic curve of gate-capacitance vs. gate-voltage is different for lower values
  - possibility to increase the gate-area by 10%

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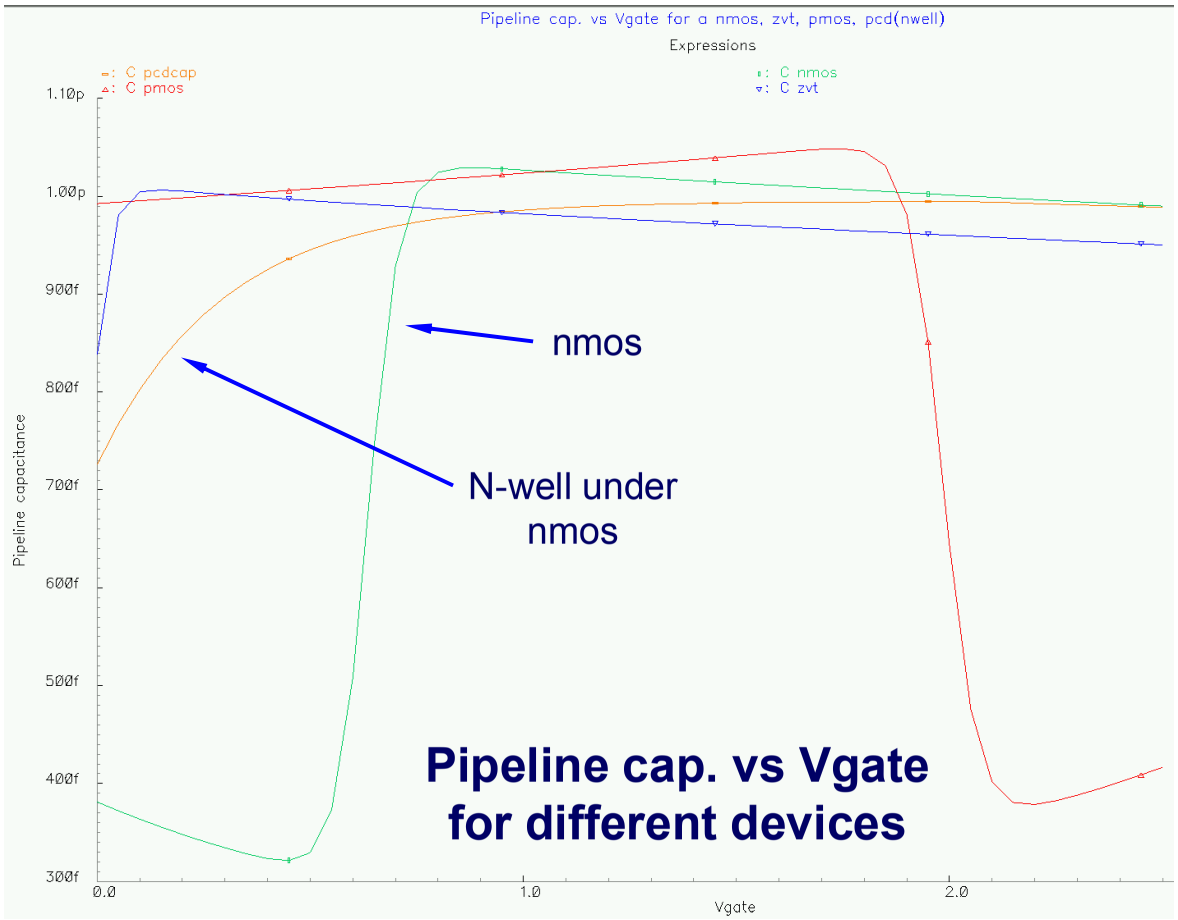
New pipeline cell

Simulation for different types of pipeline cells:

- only nmos and N-well under nmos is possible in the layout.
- without N-well:
  - cap. disappear with smaller gate voltage
- with N-well:
  - a slight larger dynamic range for positive signals (> 220.000 e^-)
- shouldn't introduce some problems, but we haven't used such kind of cell in a signal path...



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Further steps

- **Beetle 1.3 is ready to submit (old gdsII-file)**
- **If we decide to go with version 1.4:**
  - **include all modifications (pipeline, Id., parity, comparator, logo) on 1.4**
  - **➔ if the new design of the comparator is available, start with all submission tests to get a final gdsII-file (~ 3 days)**
- **Simultaneously continue with simulation of readout path of Pipeline and Multiplexer to understand the crosstalk into next channel**
  - **If problem is understood and modifications are possible, what is the next step? An additional version of a Beetle (1.5) ???**