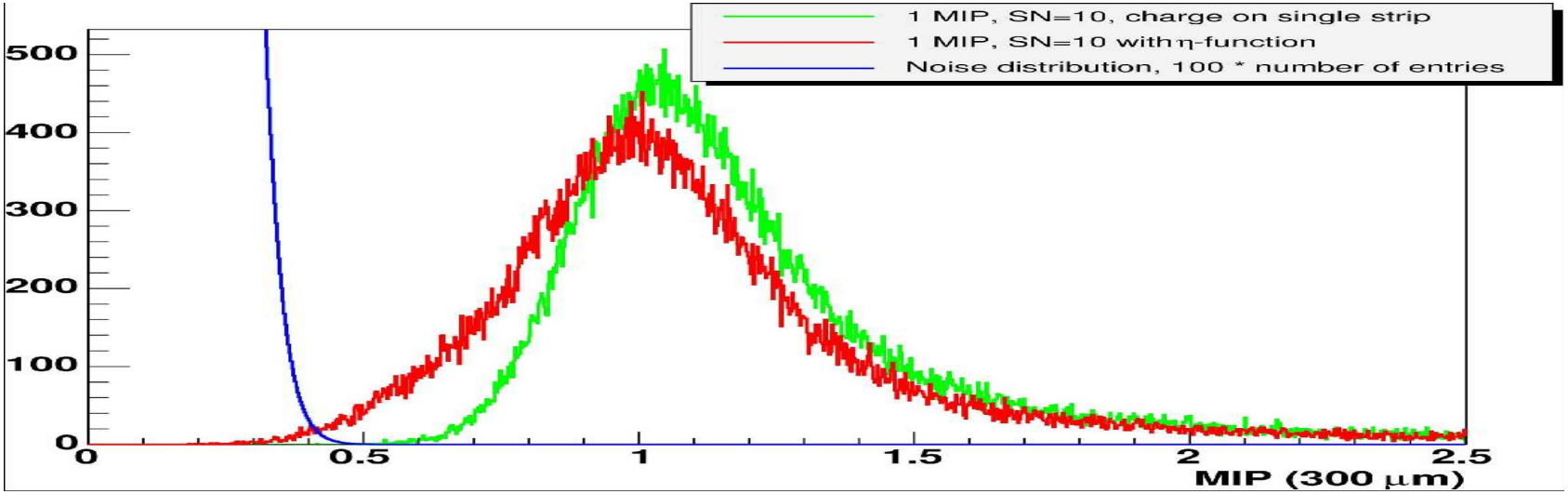
Beetle 1.3/1.4 comparator

Outline:

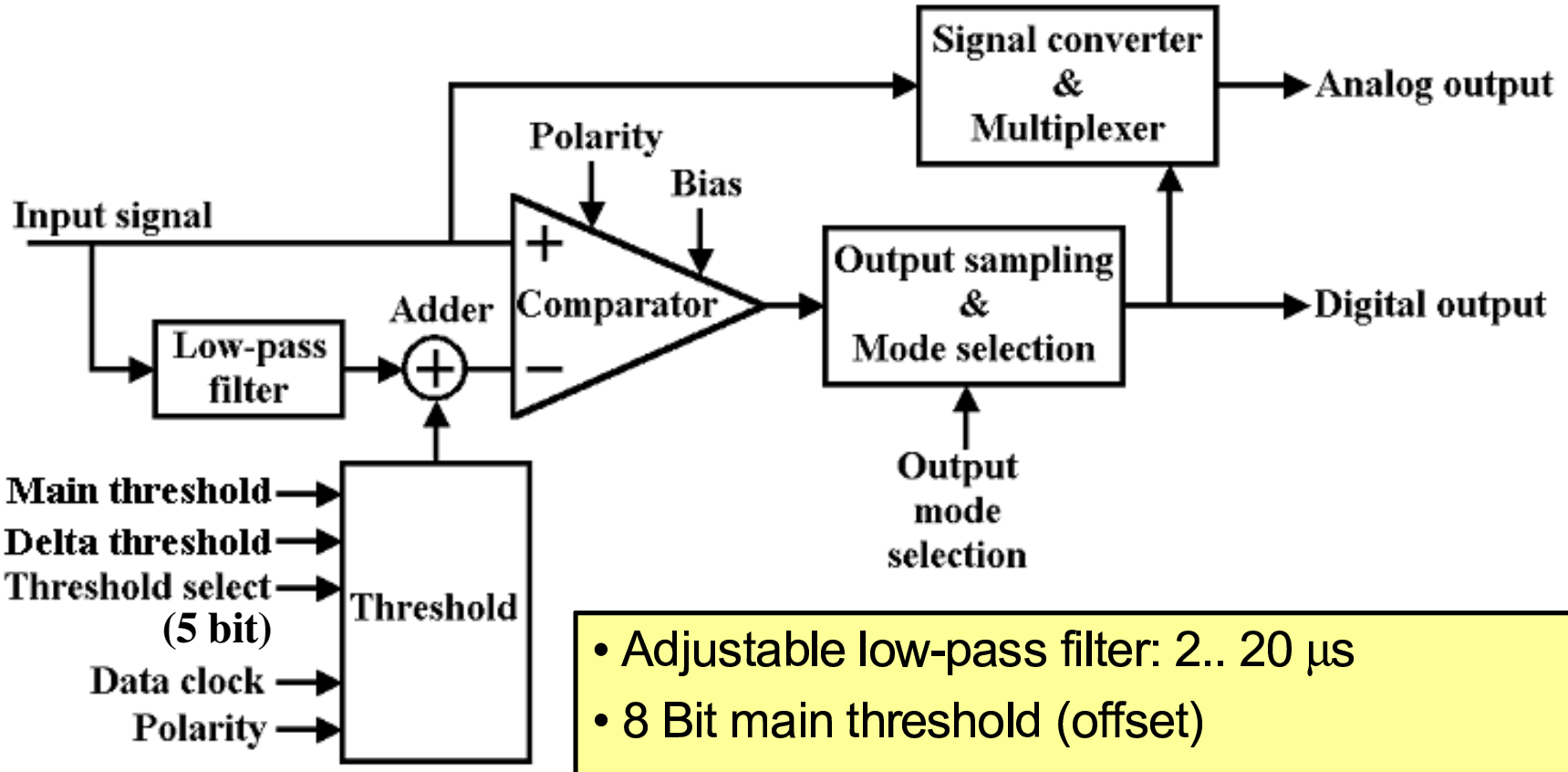
- Requirements
- Implementation
- Measurement results
- Limitation of version 1.3
- Design changes for version 1.4
- Conclusions

Requirements

- Assumptions
  - 300 μm thick silicon detectors => 22ke$^-$ per MIP
  - Minimum S/N = 10 (at end of life time)
  - Strip occupancy 1 %
- Requirements for pile-up veto
  - 100 % efficiency (charge sharing, worst case: ½ of signal on a strip)
  - Maximum contribution of noise hits: few %
  - Threshold step size better than 0.1 MIP

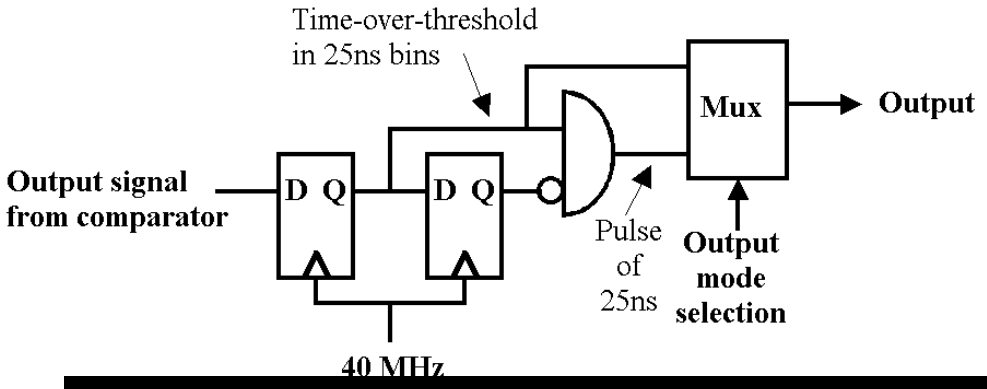


Comparator block diagram



- Adjustable low-pass filter: 2.. 20 µs
- 8 Bit main threshold (offset)
- 8 Bit delta threshold (threshold range)
- 5 Bit individual threshold
- Dual polarity
- 2 output modes: tracking or pulse mode
- Adapt digital signal to analogue pipeline level

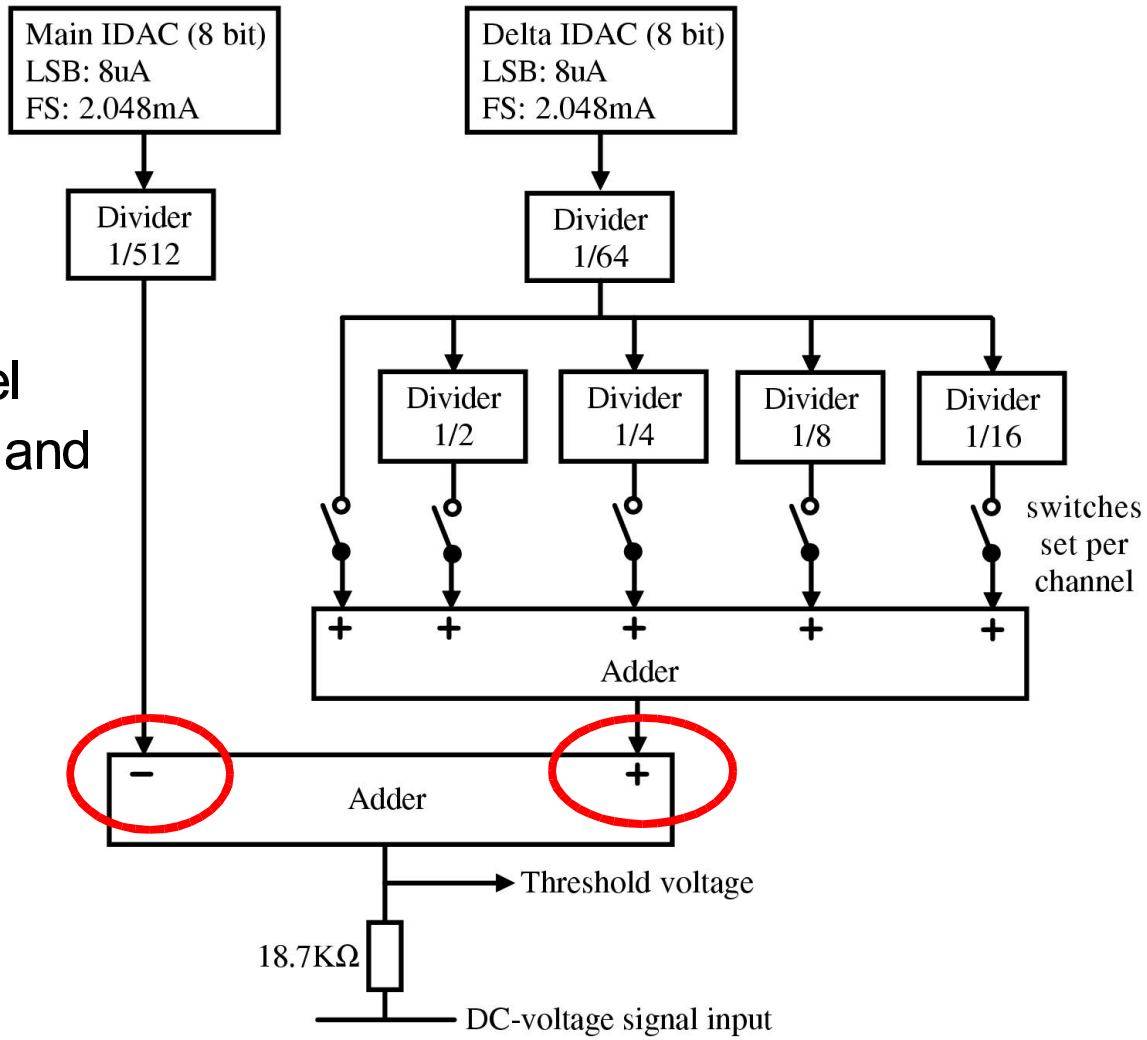
Mode selection circuit



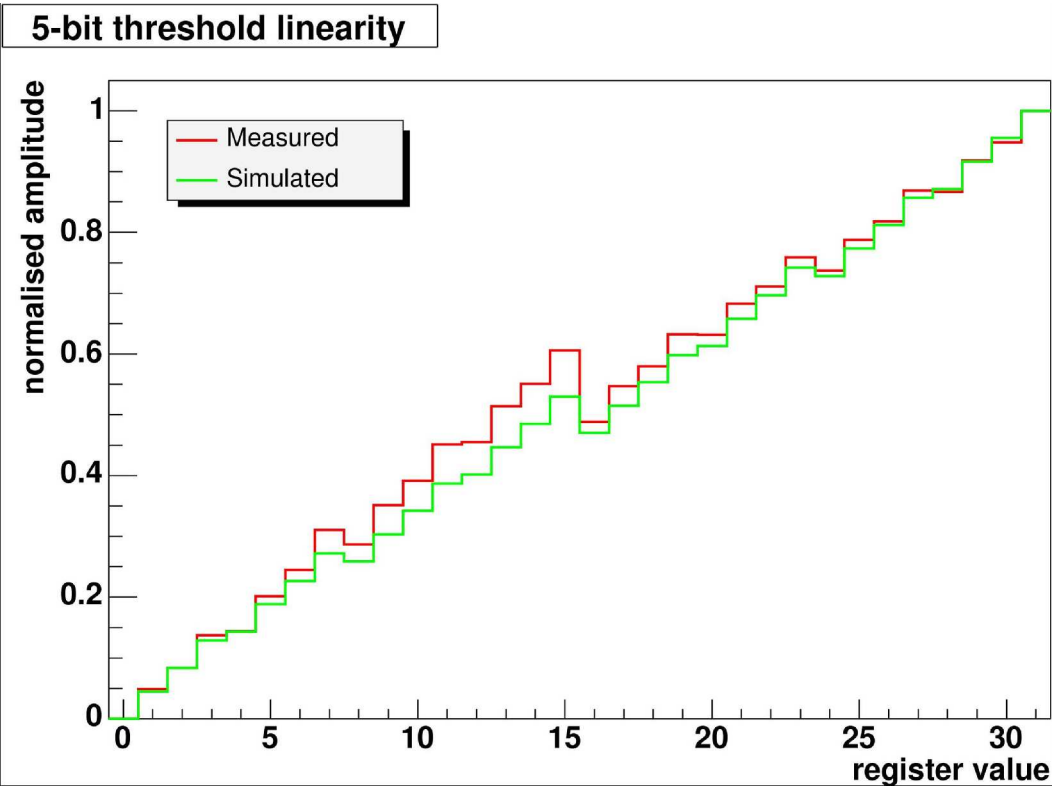
- 2 Output modes
  - Tracking mode (time over threshold)
  - Pulse mode (one clock period)

Threshold circuit

- 5 bit threshold per channel
- Opposite polarity of main and delta threshold
- Main threshold is only needed for offset compensation



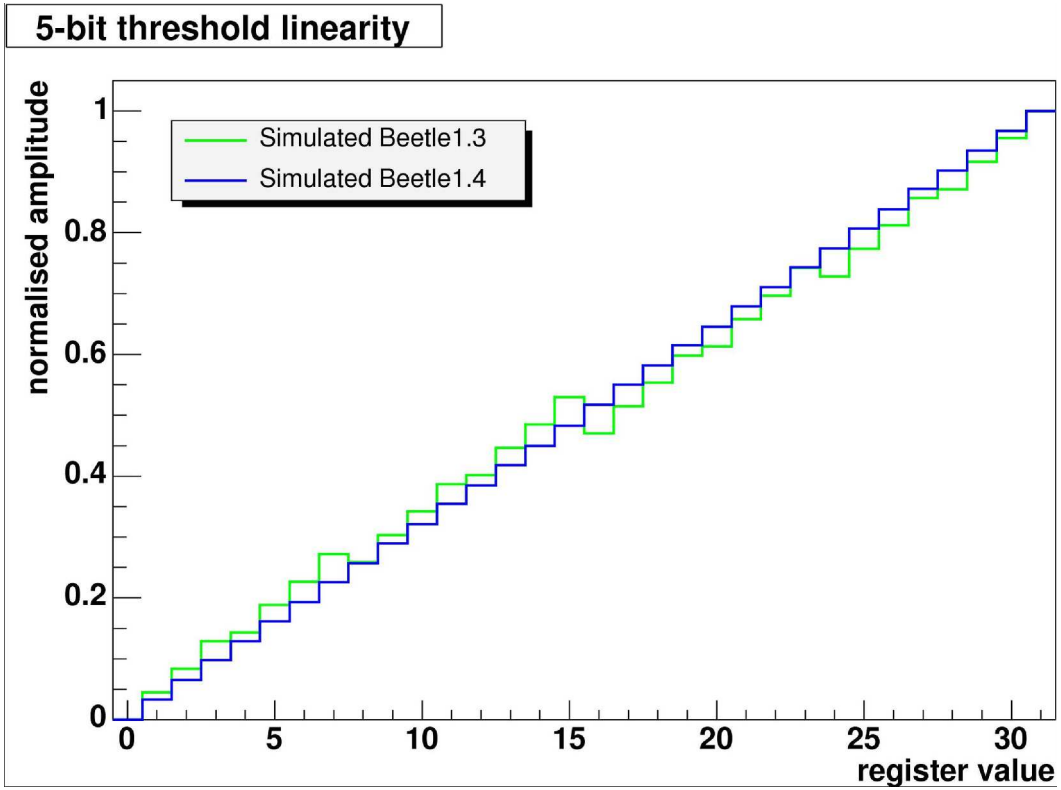
Non linearity of threshold



- Scan 5-bit threshold using external testpulse
- Curves normalized at maximum

- Non-linearity “by design”
- 5 almost identical pairs
- Largest step 85% larger than nominal

Non linearity of threshold



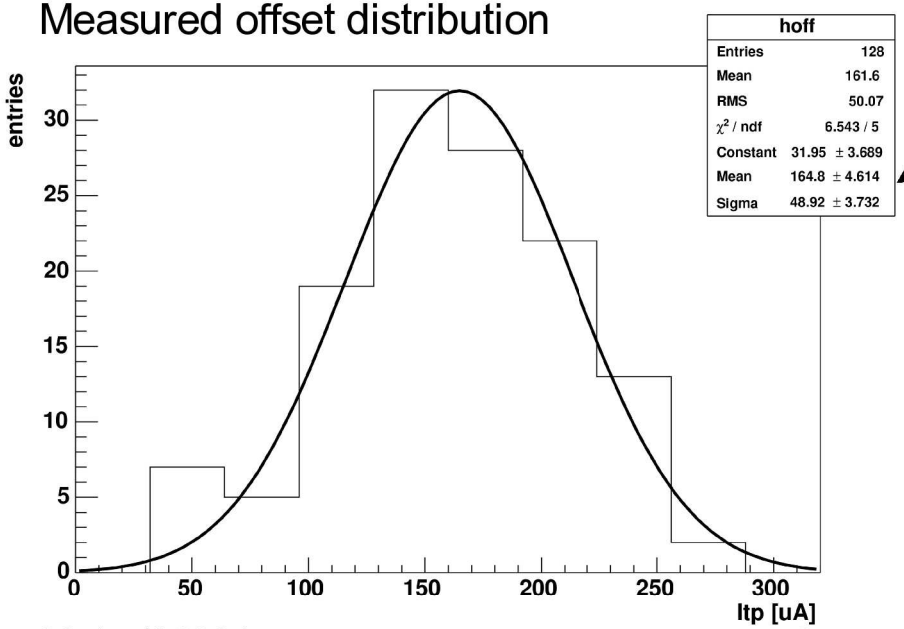
- Beetle1.4: optimized threshold current divider

Offset / threshold step size

Large offset spread in chip:

- Offset spread due to variation in process parameters (Vth)
- Cannot be improved by simple design changes
- Offset spread determines threshold range
  - Threshold step size is a direct function of the range
  - Step size obtained with Beetle1.3 ≈ 0.05 MIP (0.1 required)

Measured offset distribution



σ_{μ} = 49 A Itp = 49 * 110 e-

σ = 5.4ke-

Offset range = $2*3\sigma$ = 32.4ke-

= ~1.5MIP

Step size = 1.5MIP / 26 steps

≈ 0.05 MIP

Lower threshold limit

In the following, we choose the delta thresholds such that the effective threshold is the same for all 128 channels.

GOAL: Find the lowest possible threshold.

For this, we fire a large test-pulse on a selected number of channels; the test-pulse inputs of the remaining channels are masked.
The number of selected channels varies: 1, 4, 8, 16 …..

We call a threshold setting OK if the number of outputs that fires equals the number of channels that receives a test-pulse.

We lower the threshold step by step, until the OK condition fails.
At that point we increase the threshold again until the OK situation comes back.
This latter threshold value is labeled stable operation.

Threshold limit: positive polarity

# test-pulse inputs enabled	Min. possible threshold for OK condition (μA Itp)	Min. possible threshold for stable operation (μA Itp)
1	42	55
2	42	55
4	42	55
8	47	55
16	47	55
32	52	55
64	55	55

- No silicon detector
- Values in table are not very precise
- Below OK condition, the chip starts to oscillate
- Switching off pre-amp or shaper stops oscillation
- Coupling via ground / substrate / Vdd

Threshold limit: negative polarity

# test-pulse inputs enabled	Min. possible threshold for OK condition (μA Itp)	Min. possible threshold for stable operation (μA Itp)
1	68	68
2	68	68
4	68	68
8	71	71
16	74	74
32	103	103
64	130	130

- No silicon detector
- Values in table are not very precise
- No oscillation observed
- Below OK condition, all outputs fire simultaneously
- This indicates fast feedback, i.e., in the comparators
- Strong dependence on # test-pulse inputs enabled

Threshold limit with silicon

With silicon, the lower threshold limit increases by 30 .. 40 μA (Itp)
This is expected because:

- Input capacitance reduces peak amplitude (in mV) of the front-end.
- The margin (in mV) inside the chip is fixed.

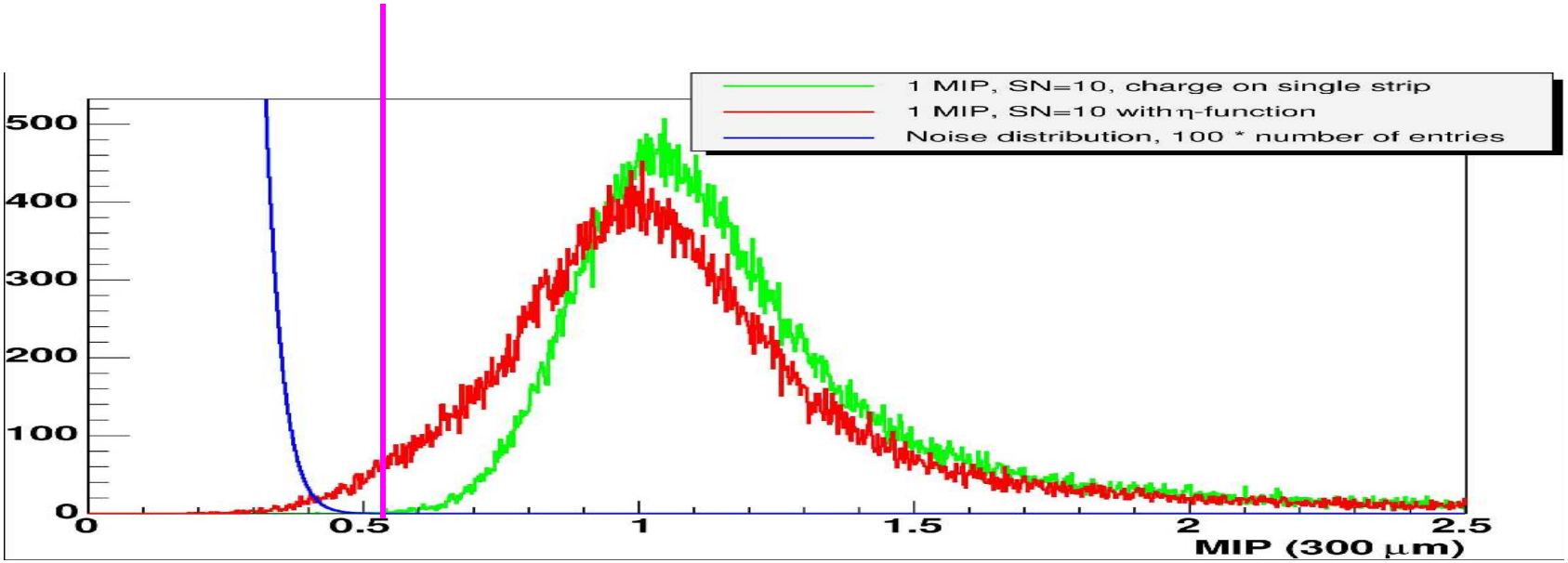
Summary of results

Lower threshold limit for 8 test-pulse inputs enabled (“8 tracks”)

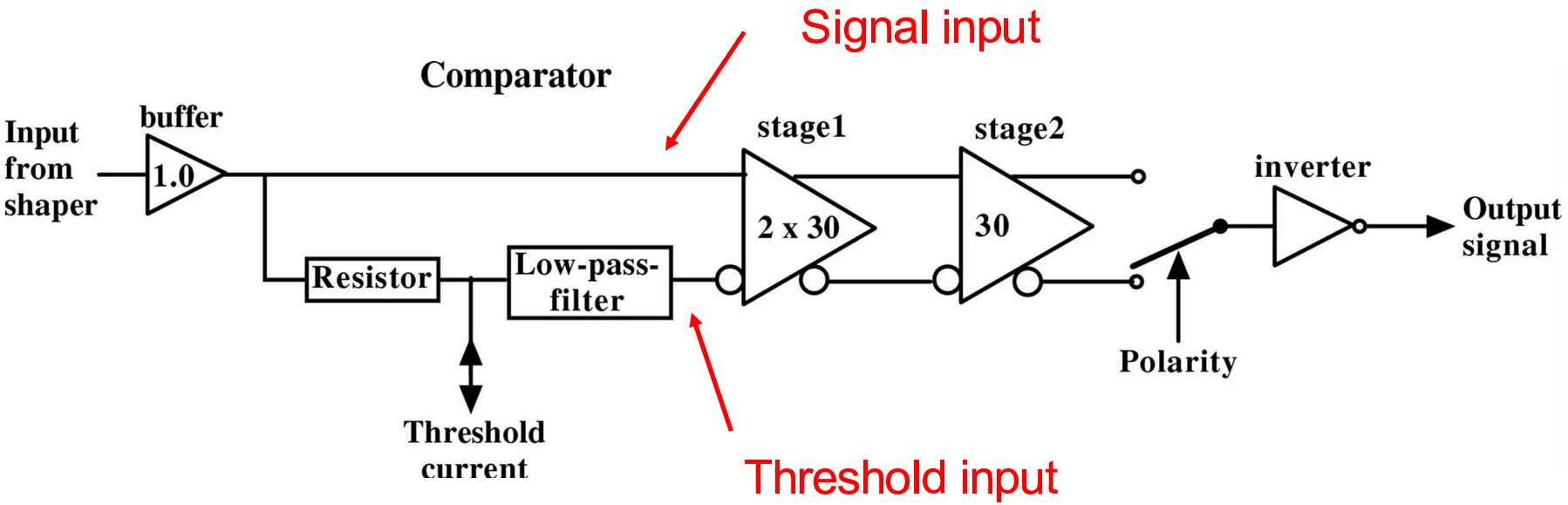
	Positive mode	Negative mode
No silicon	6.1 ke$^-$	7.8 ke$^-$
Silicon	9.9 ke$^-$	11.6 ke$^-$ (0.53MIP)

The numbers in the table are not accurate

Note: a threshold of 0.53 MIP gives 3..4 % inefficiency (no CM noise)

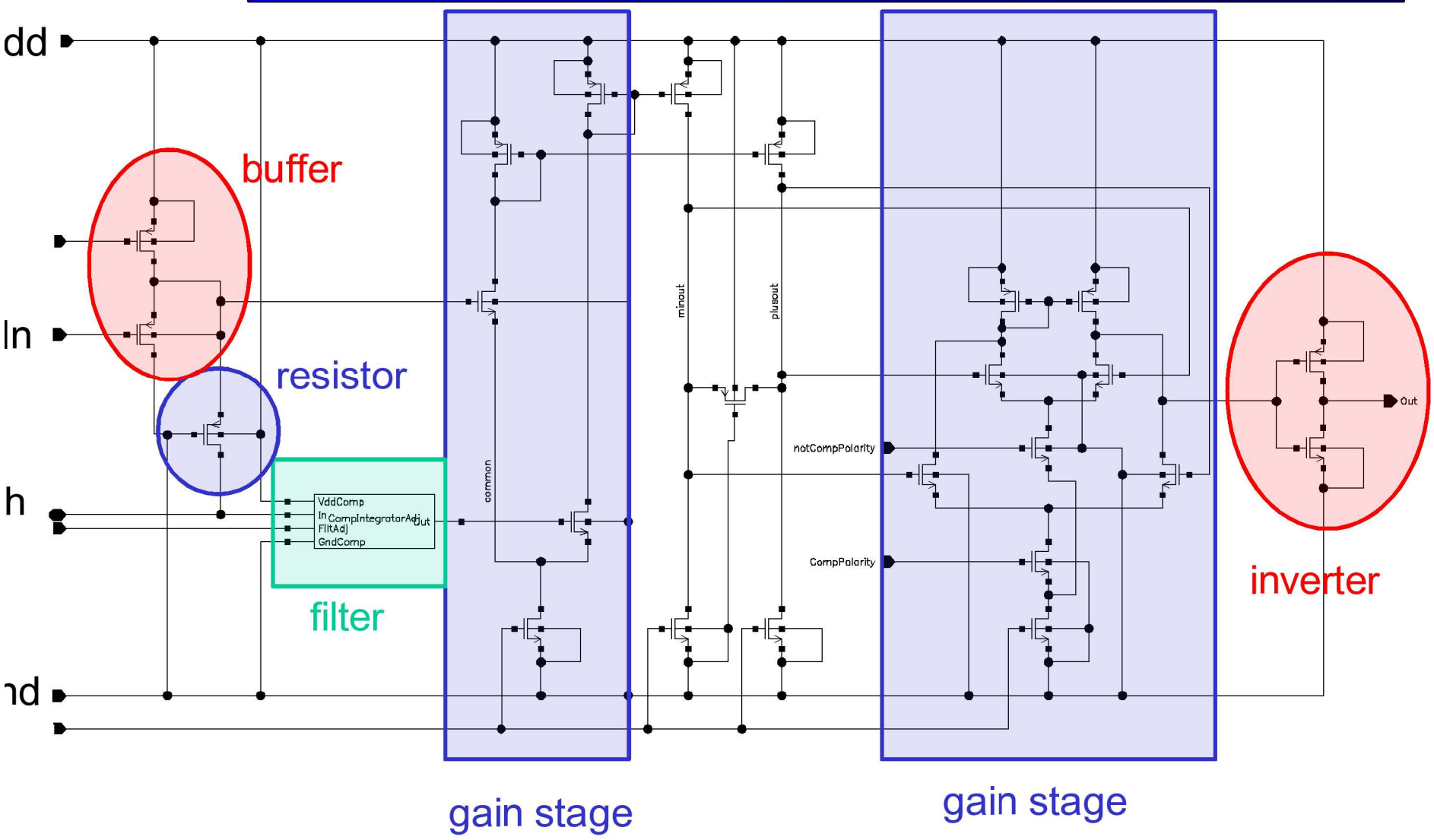


Comparator of Beetle1.3

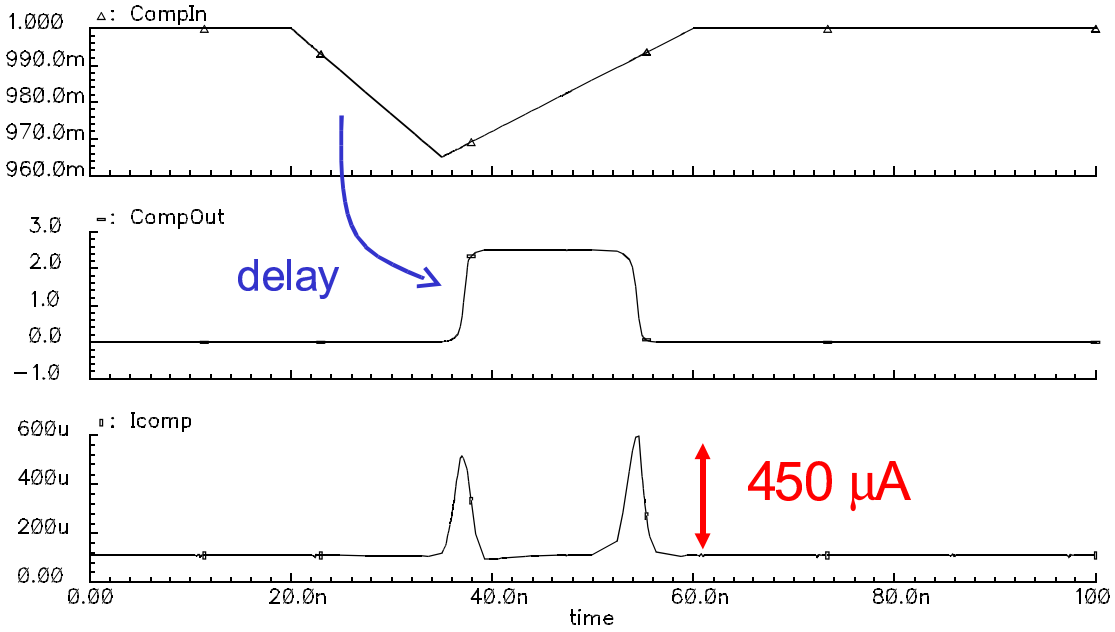


- The polarity mode is either: Positive (p-on-n det.) or Negative (n-on-n det.).
- The polarity of the threshold current is coupled to polarity switch.

Comparator details



Switching current



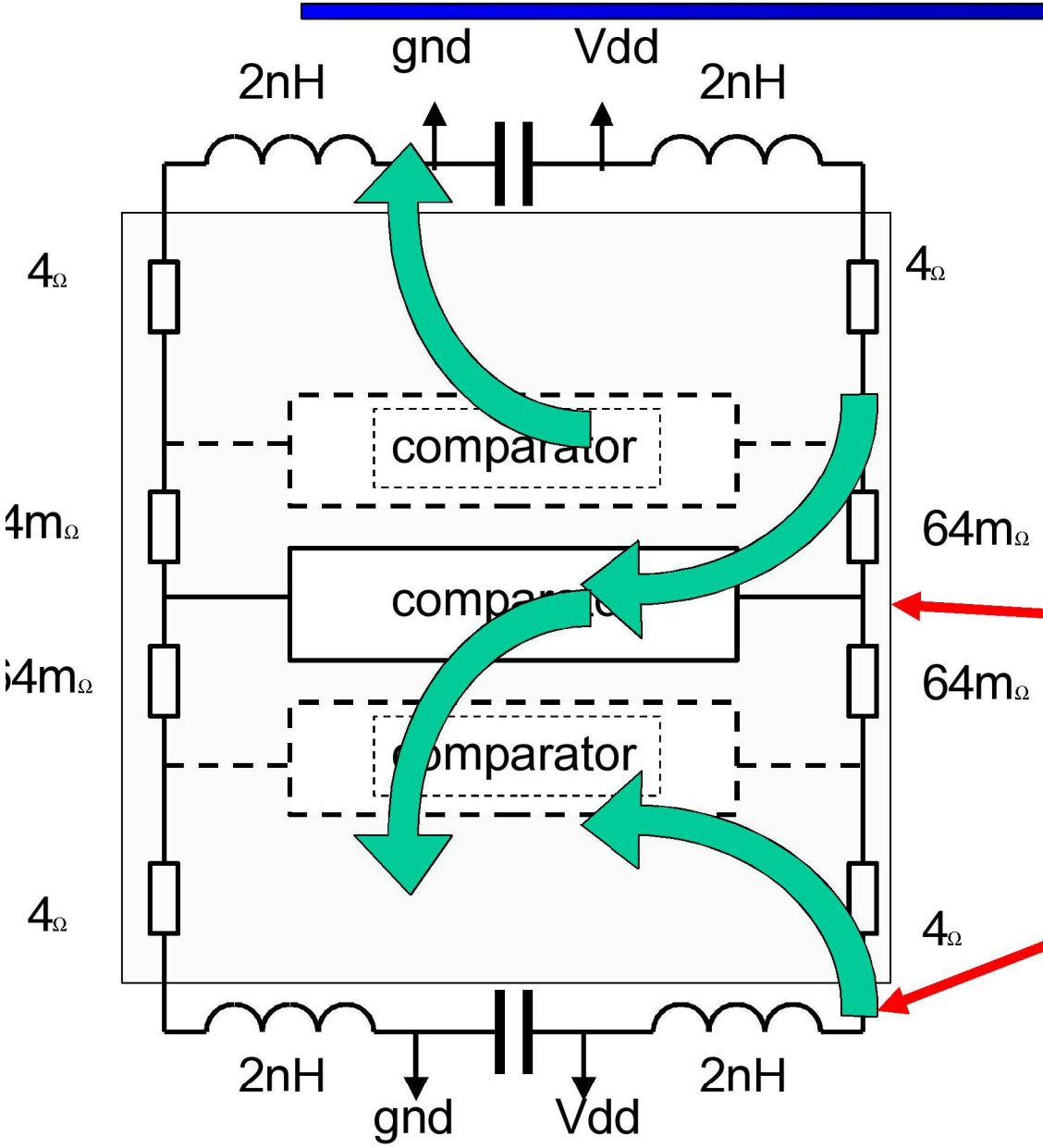
Signal input

Comparator output

Current through inverter

- Large current peaks in the power lines (450 µA) when inverter switches.
- The current is almost equal for rising and falling edge => slow switching.
- About 1 pC of charge flows through the power line

Power routing in chip



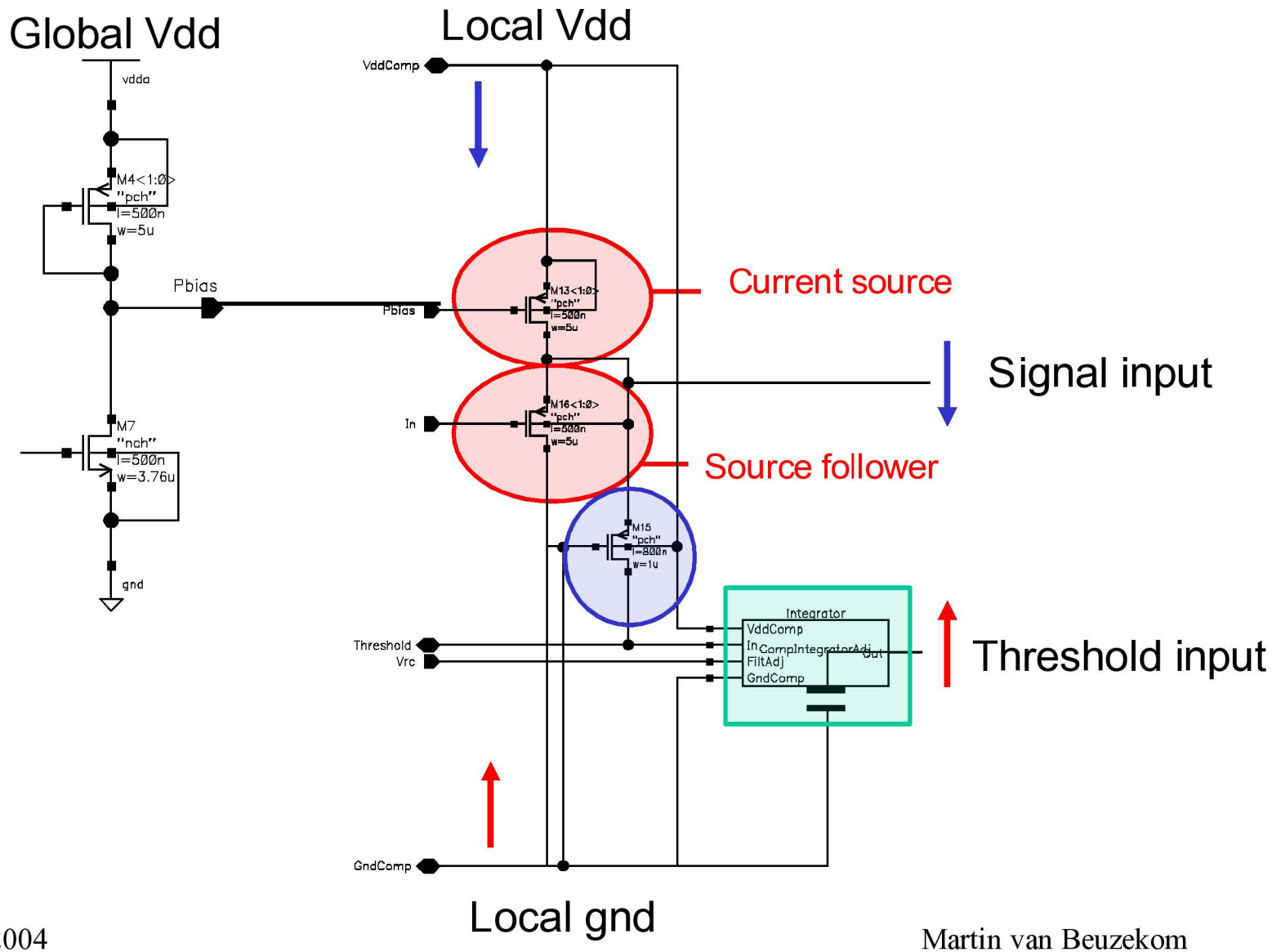
Impedance of power lines is not negligible, causing voltage spikes:

$450\ \mu A * 2\ \Omega \approx 1mV$
= 650e-

When inverter switches:
"local" Vdd drops,
"local" gnd rises

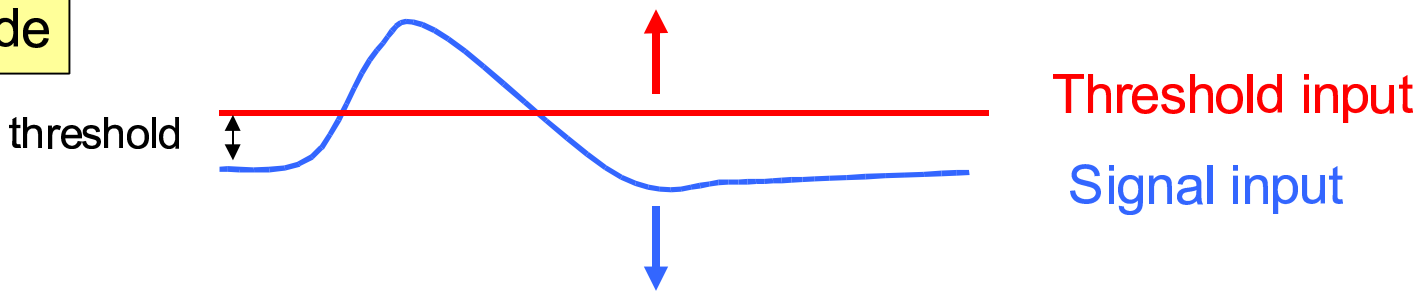
But: threshold and bias circuits refer to "global" Vdd

Effect of voltage drop



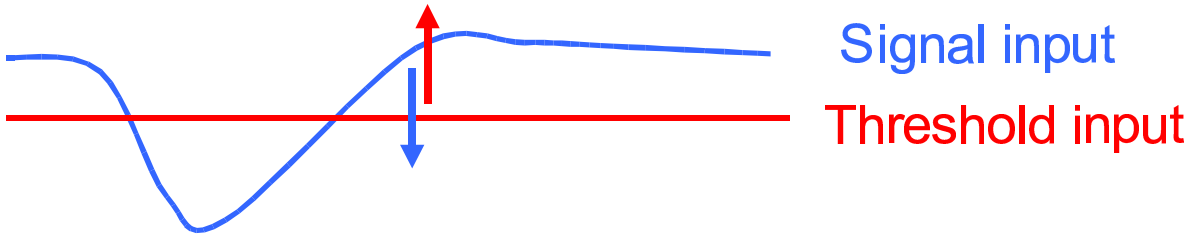
Change of threshold

Positive mode



⇒ Switching of inverter increases threshold
⇒ Expected: negative (no) dependence on #channels switching
⇒ Observed: weak positive dependence (table on sheet 10)

Negative mode



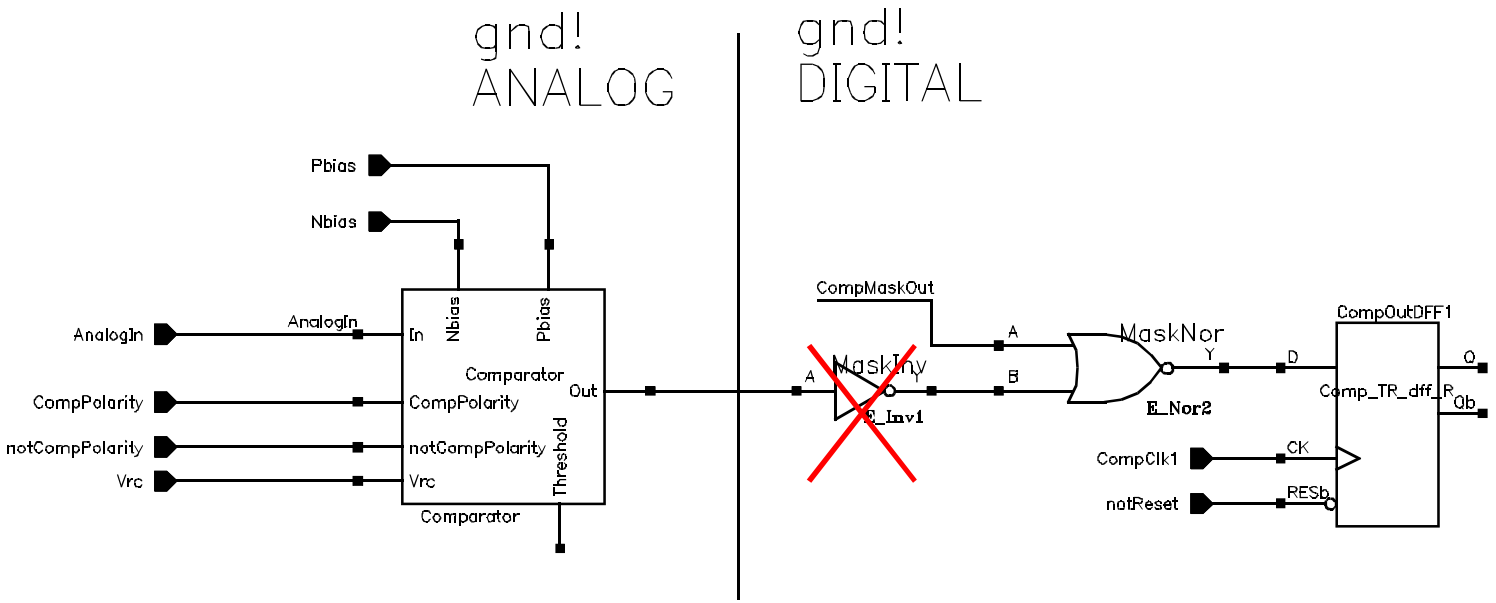
⇒ Switching of inverter decreases threshold
⇒ Expected: positive dependence on #channels switching
⇒ Observed: strong positive dependence (table on sheet 11)

Change of threshold

- Observed effects cannot be explained by coupling in comparator only.
- Front-end plays a role as well.
- But: simple simulation model of noise coupling to front-end gave no consistent results

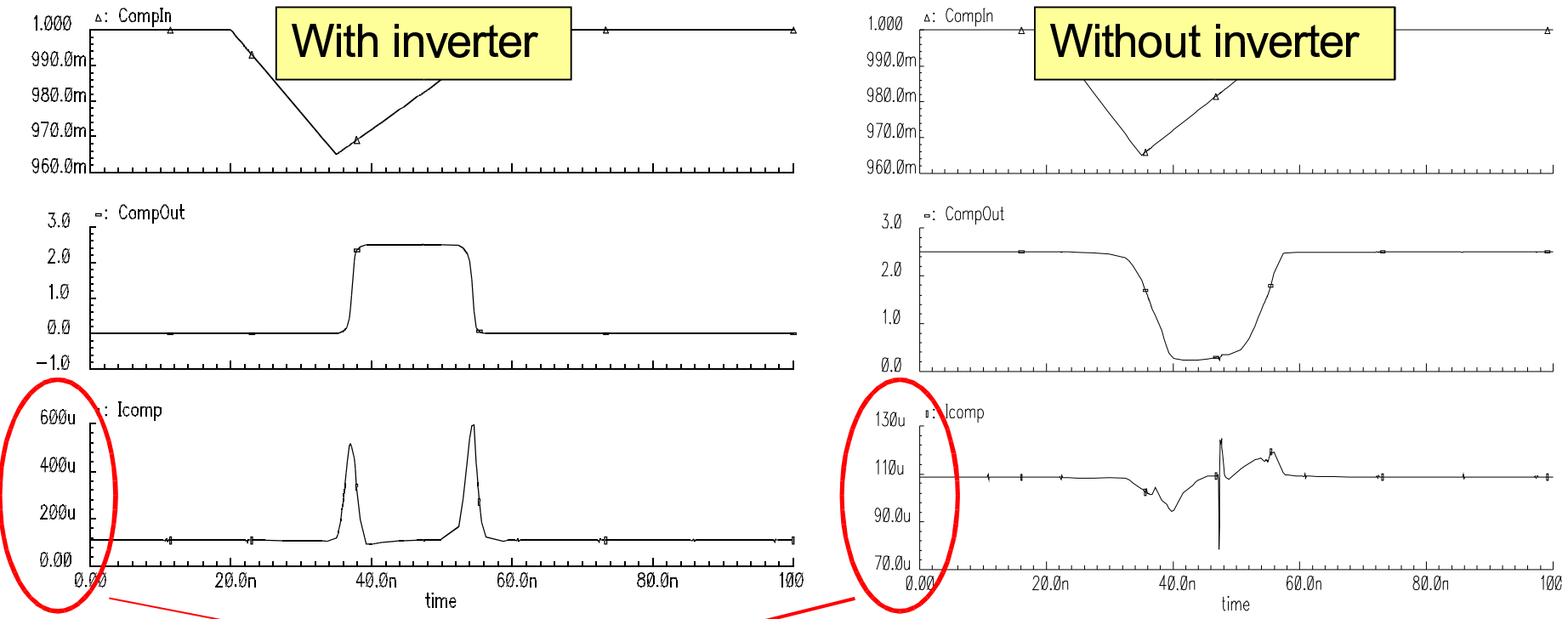
Modifications (1)

- Remove inverters from comparator and from logic at output



Beetle1.3 configuration

Simulation after modification

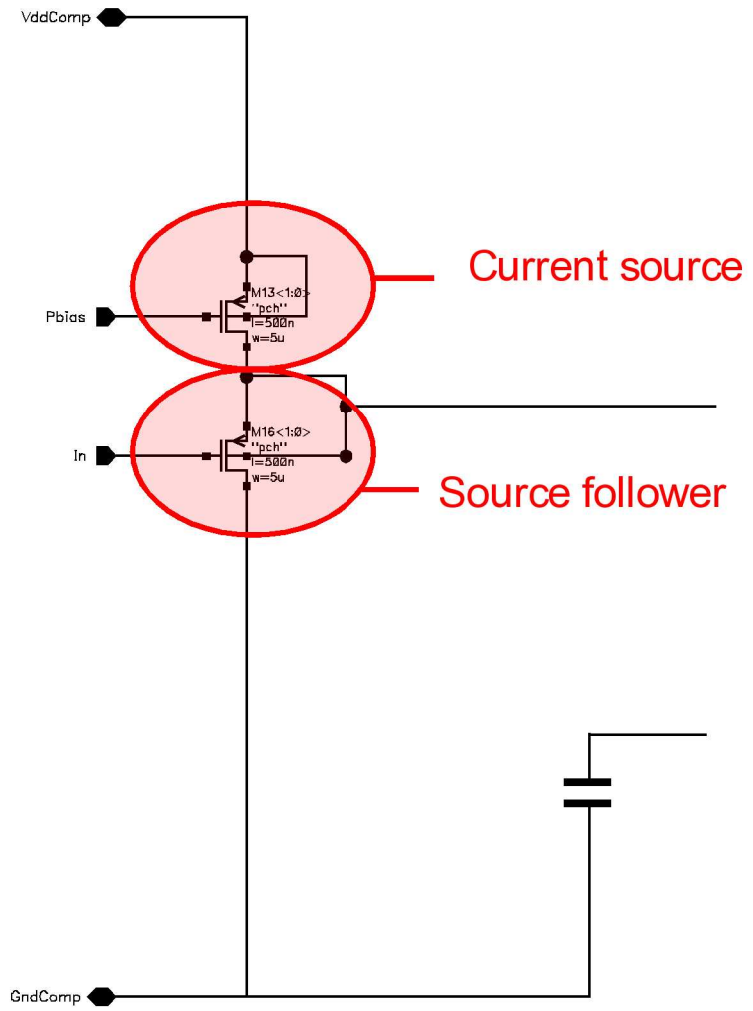


Scales differ by factor 10

- Peak currents are strongly reduced
- Charge flowing through power lines < 70 fC

Modifications (2)

- Change dimension of source follower and current source to reduce the effect of power supply variations.



Conclusions

Beetle1.3:

- ✪ Functional behavior of comparator is OK
- ✪ Comparator offsets are under control
- ✪ Threshold step size is within specification
- ✭ Use of the comparators with positive pulses (p-on-n detector) can lead to oscillations => high threshold needed.
- ✭ The lowest possible threshold for n-on-n detectors is too high.

Beetle1.4:

- Noisy inverter of comparator is removed
- Power supply sensitivity is reduced by new dimensions of input buffer
- Threshold linearity is improved