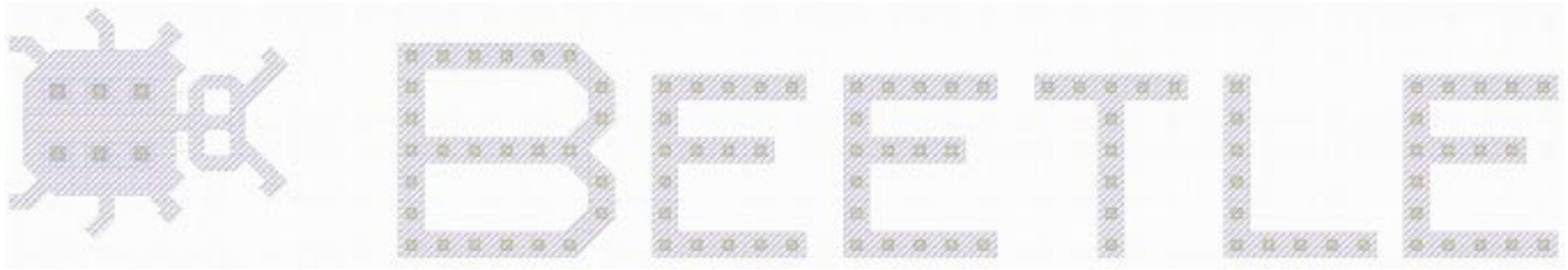

Submission and Production Plans

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IBM CMOS6sf Constraints

IBM Technology:

- 20cm (8") wafers
- about 685 beetle-sized chips

Engineering Run:

- Cost ~120 kEUR
- Max. 6 wafers
- 2 wafers guaranteed minimum
- Striping optional

Poduction Run:

- Cost ~110 kEUR
- Only with engineering masks
- Only multiples of 48 wafers

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A little Math.....

Assumption: Yield=85%

		Chips	Chips	Chips
	Wafers	1 Version	2 Versions	3 Versions
1 Wafer	1	600	300	200
1 Engineering run	6	3600	1800	1200
1 Production Lot	48	28800	14400	9600

Dates and available Chips

	Optimistic	Late			VELO	ST	VETO
				01.04.2004	20 (1.3)	60 (1.3)	2 (1.3)
Submission of Engineering Run	15.05.2004	01.06.2004					
				01.06.2004		290	16 (1.3)
Wafers back	15.08.2004	15.09.2004					
1st Wafer cut	01.09.2004	01.10.2004	~300 (200..600) untested Chips available				
5 Wafers tested	15.09.2004	01.11.2004					
5 Wafers cut	01.10.2004	15.11.2004	~1500 (1000..3000) tested Chips avail.	01.10.2004	250	610	20
Production Order	15.09.2004	01.11.2004	Current turn-around ~18 weeks (w. increasing tendency)				
Deilvery of 48 wafes	01.02.2005	01.06.2005		01.02.2005	1200	2000	
				01.05.2005	1200		128

All numbers are incremental
Chip request should be related to the "optimistic" planning, since both assume no unforseen delays