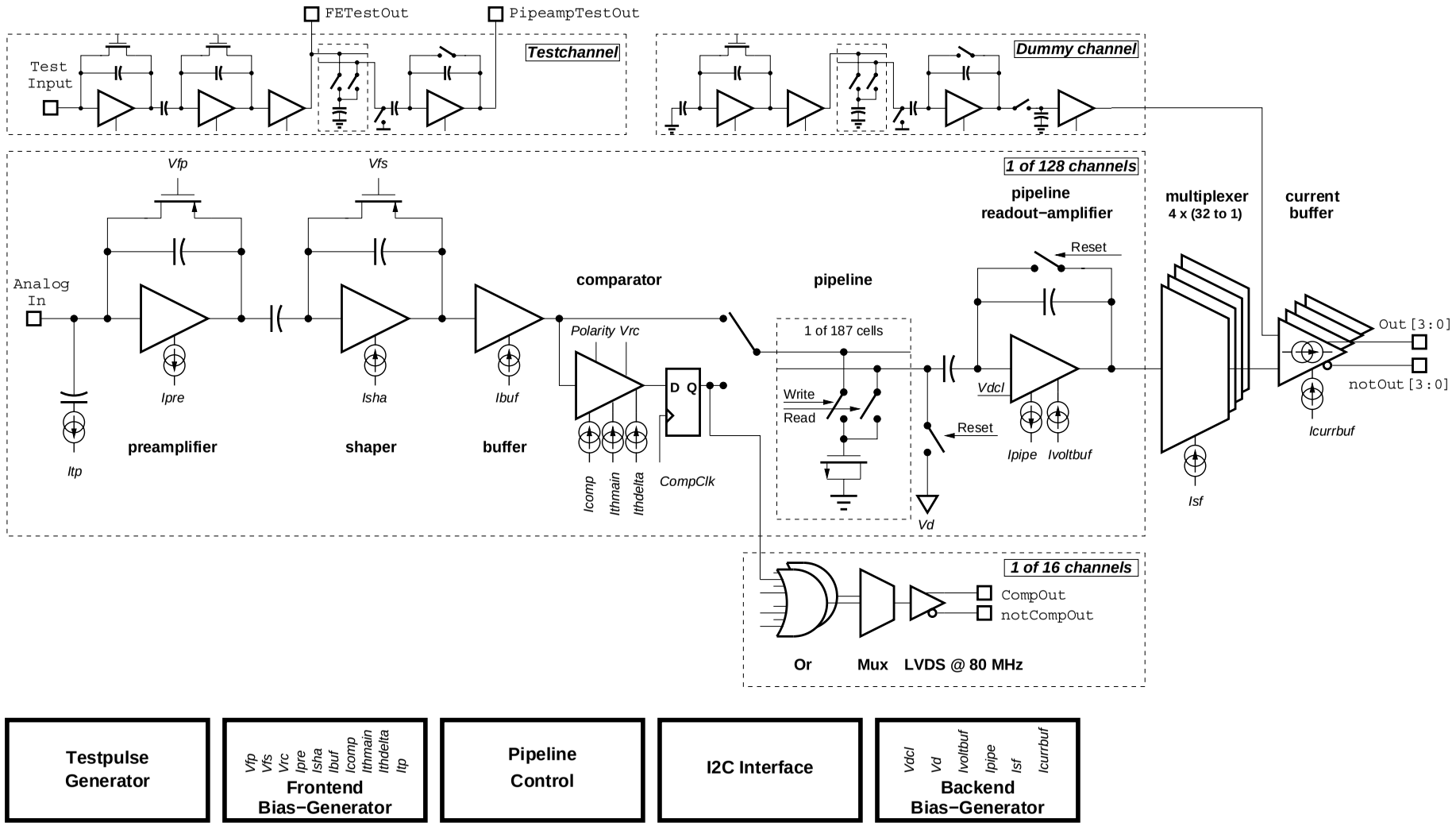
Beetle 1.2 Blockschematic



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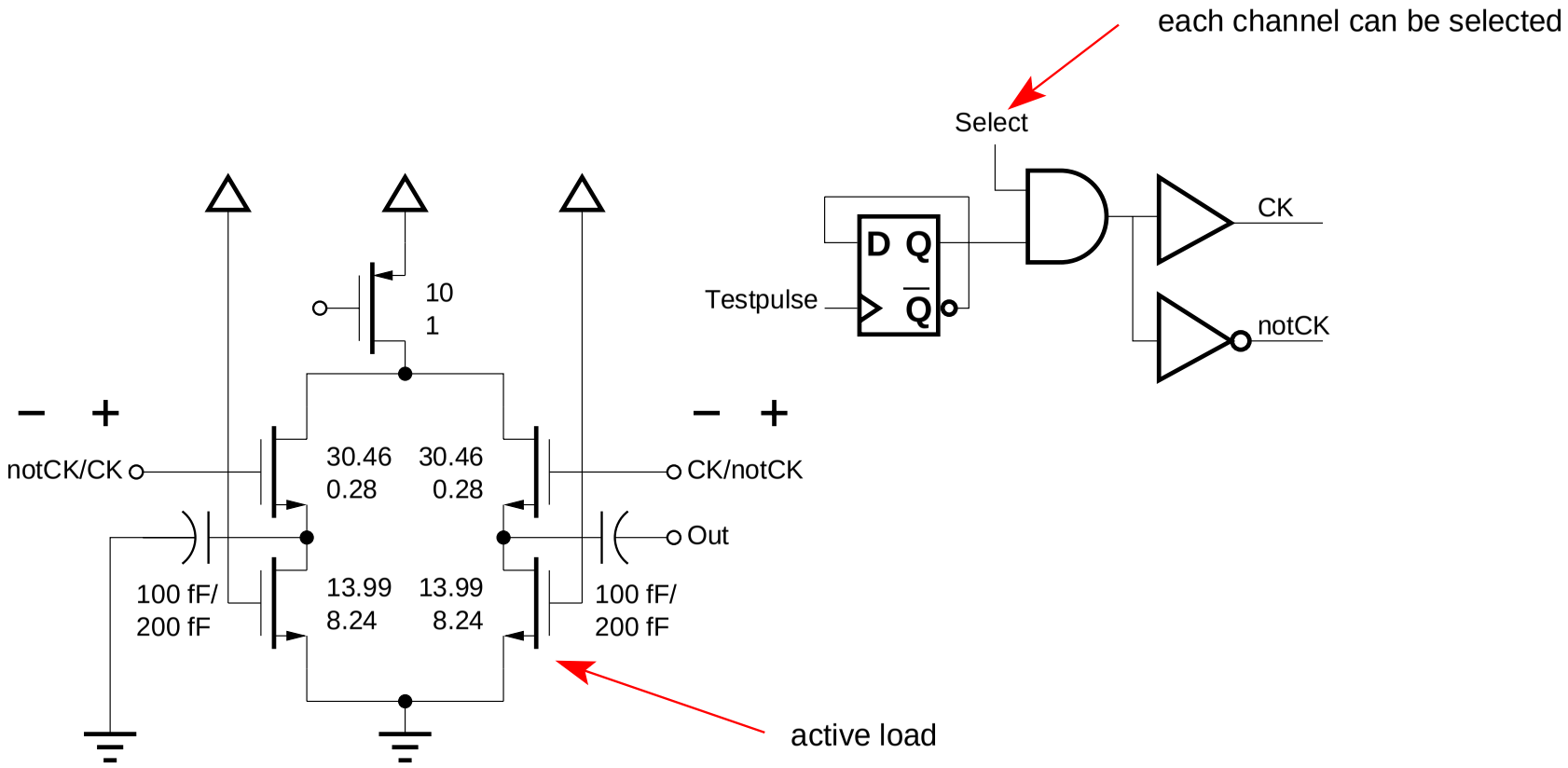
Testpulse



four different testpulse types are generated

steps correspond to +2, +1, −1, −2 times the input signal amplitude

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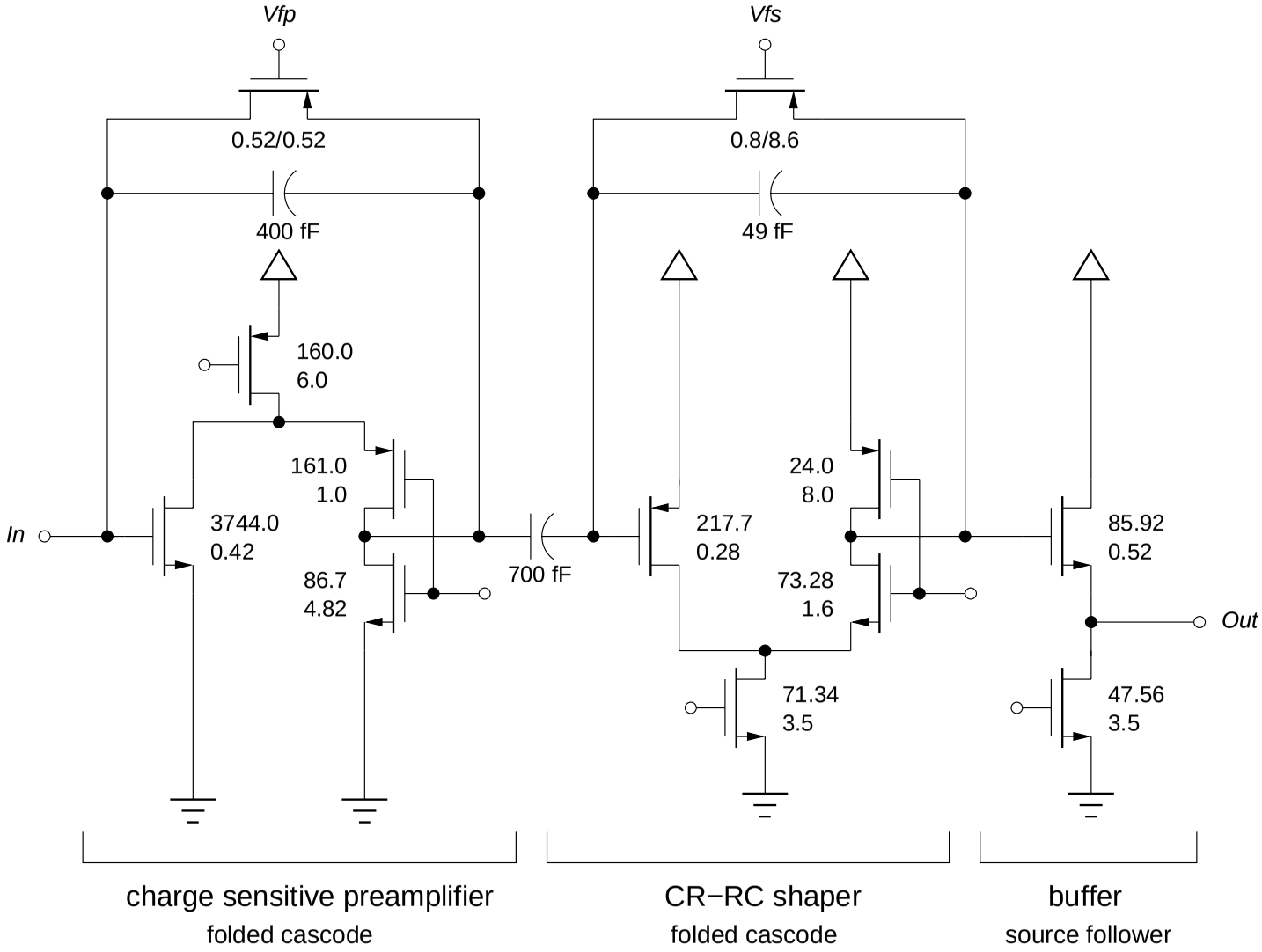
Frontend



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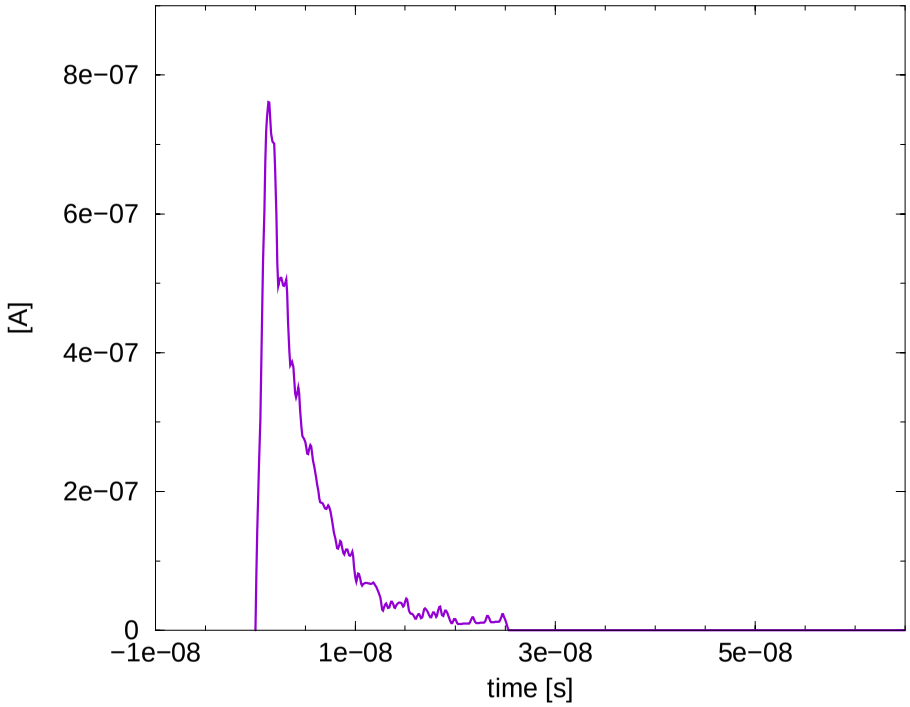
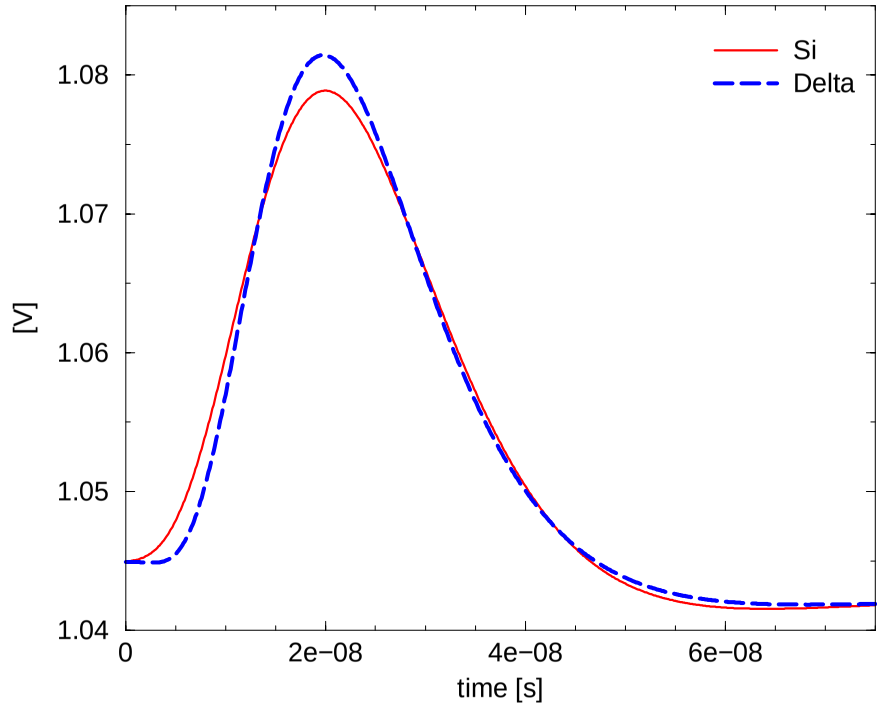
Transient response of FE





Simulated primary current pulse of a silicon sensor

P. Sievers

Transient response of the front−end

- delta−shaped pulse (dashed line)
- current pulse (solid line)

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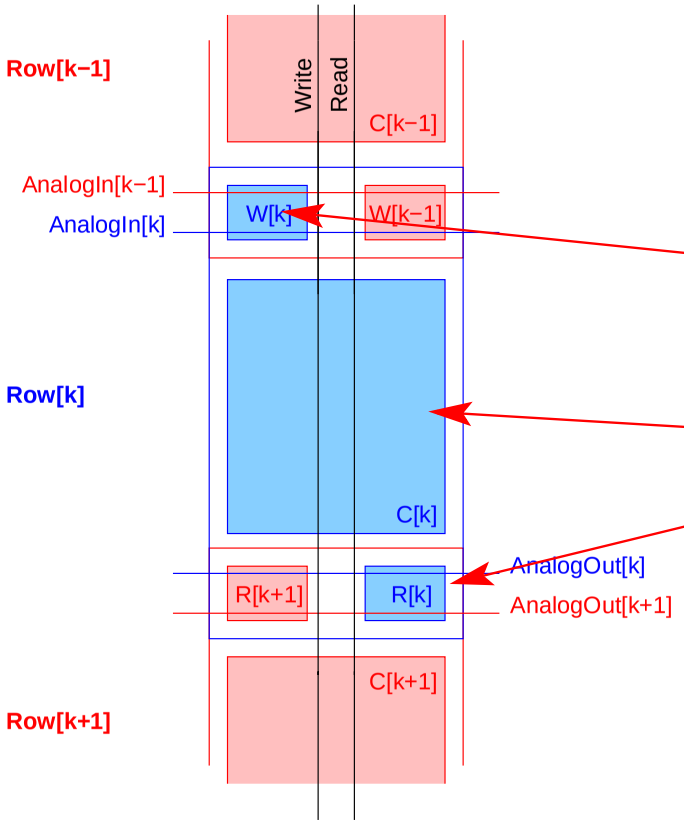
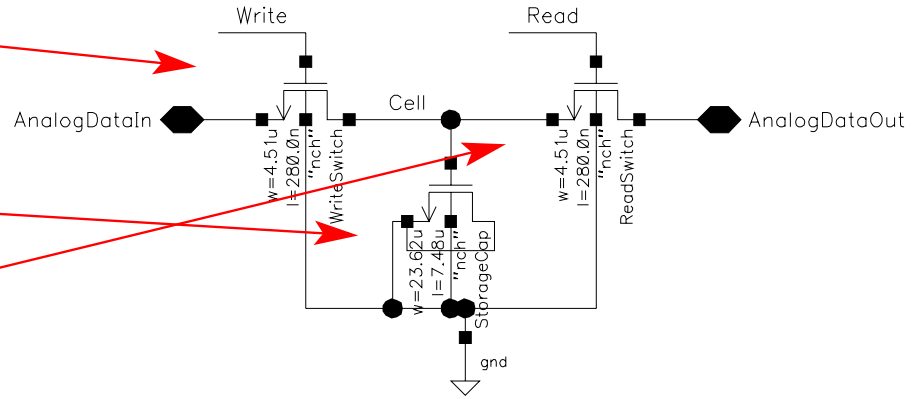
Pipeline cell





corresponding schematic

Layout of one pipeline storage cell with the adjacent cells in the same column

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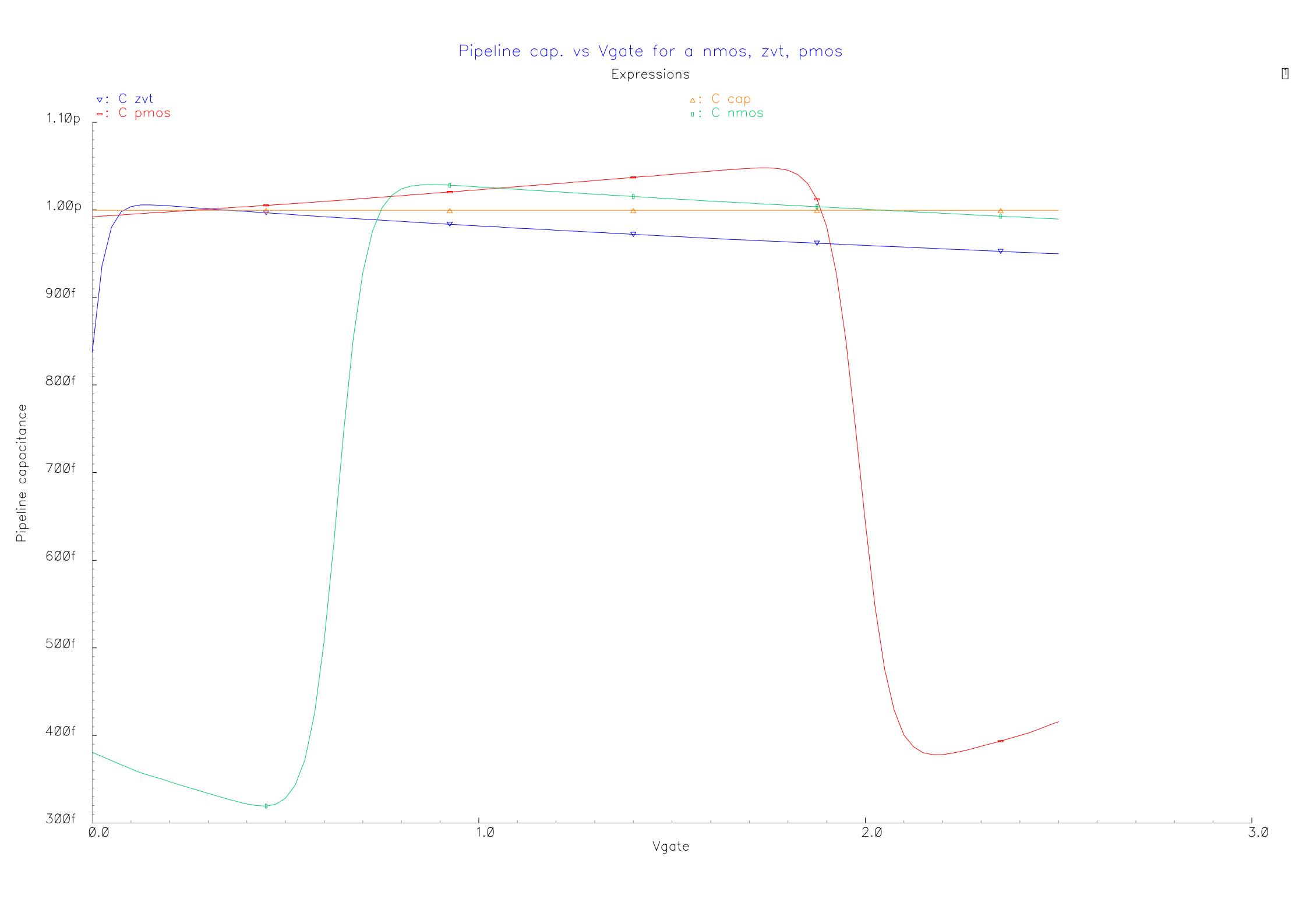
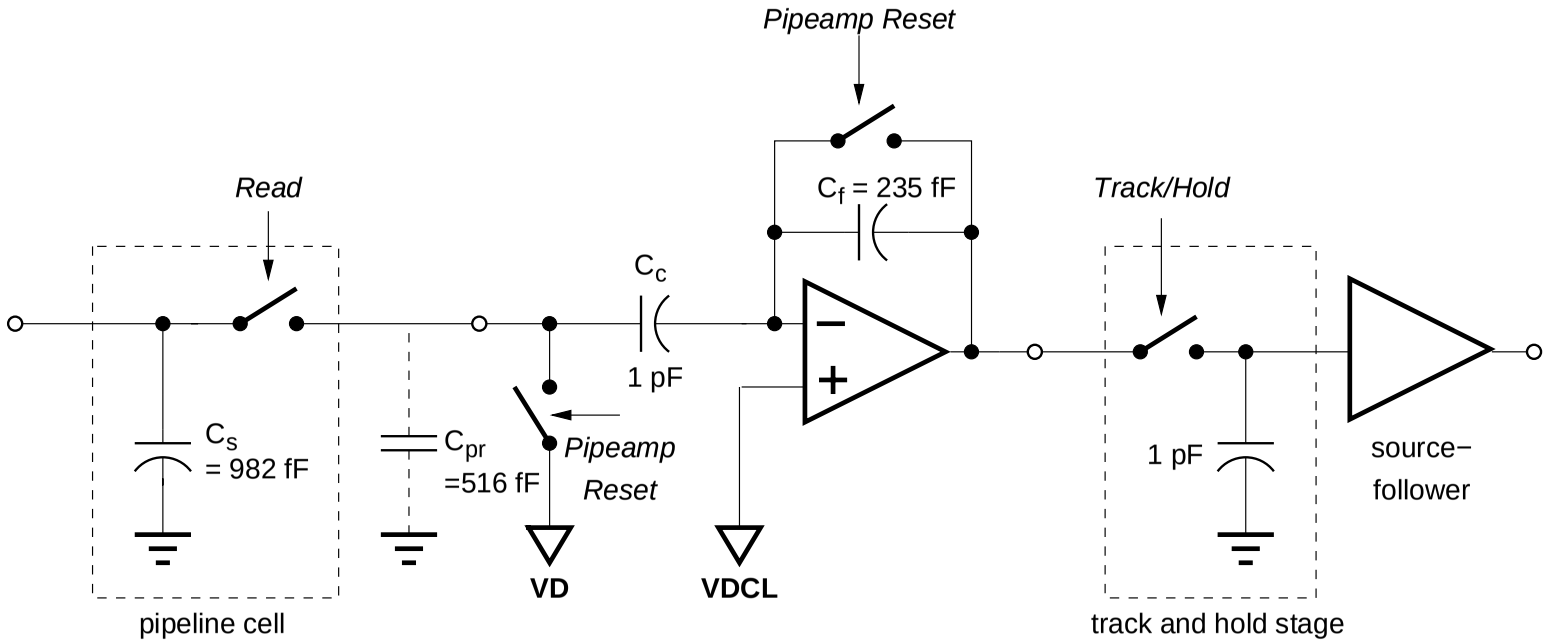

Pipeline cap. vs Vgate for a nmos, zvt, pmos
Expressions
▽: C zvt
▭: C pmos
△: C cap
▯: C nmos
1.10p
1.00p
900f
800f
700f
600f
500f
400f
300f
Pipeline capacitance
0.0
1.0
2.0
3.0
Vgate

Pipeline readout



resetable charge sensitive amplifier

AC−coupled to the pipeline

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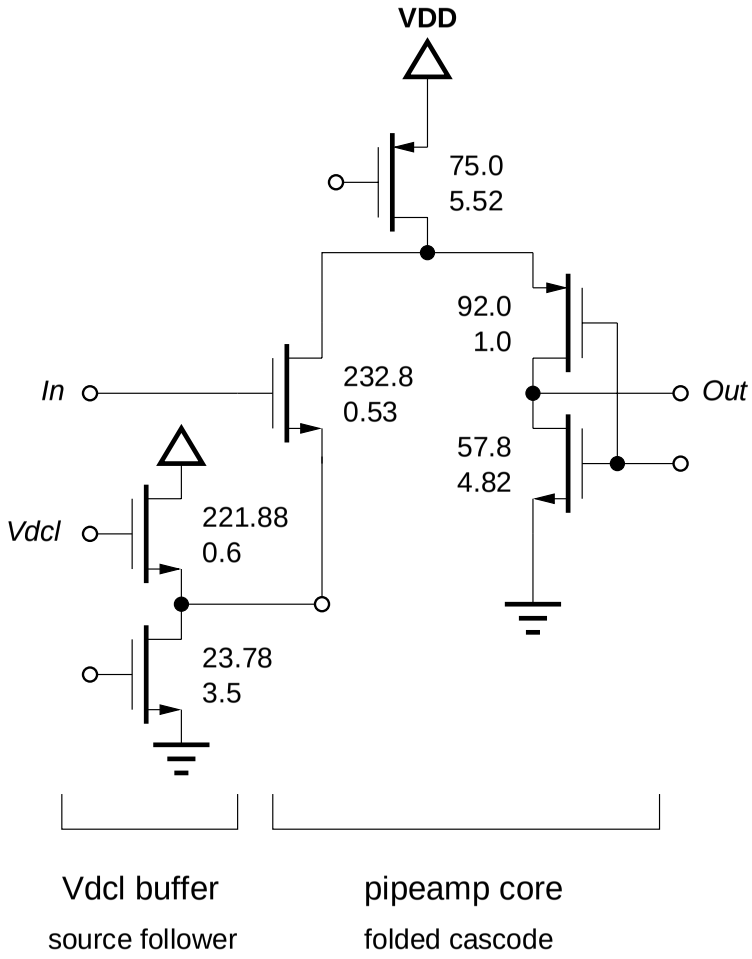
Pipeline amplifier



- Pipeamp is reset in between two readouts (to Vd)
- Vdcl bias voltage works as the non−inverting input of the amplifier
- Vdcl node is buffered in each channel

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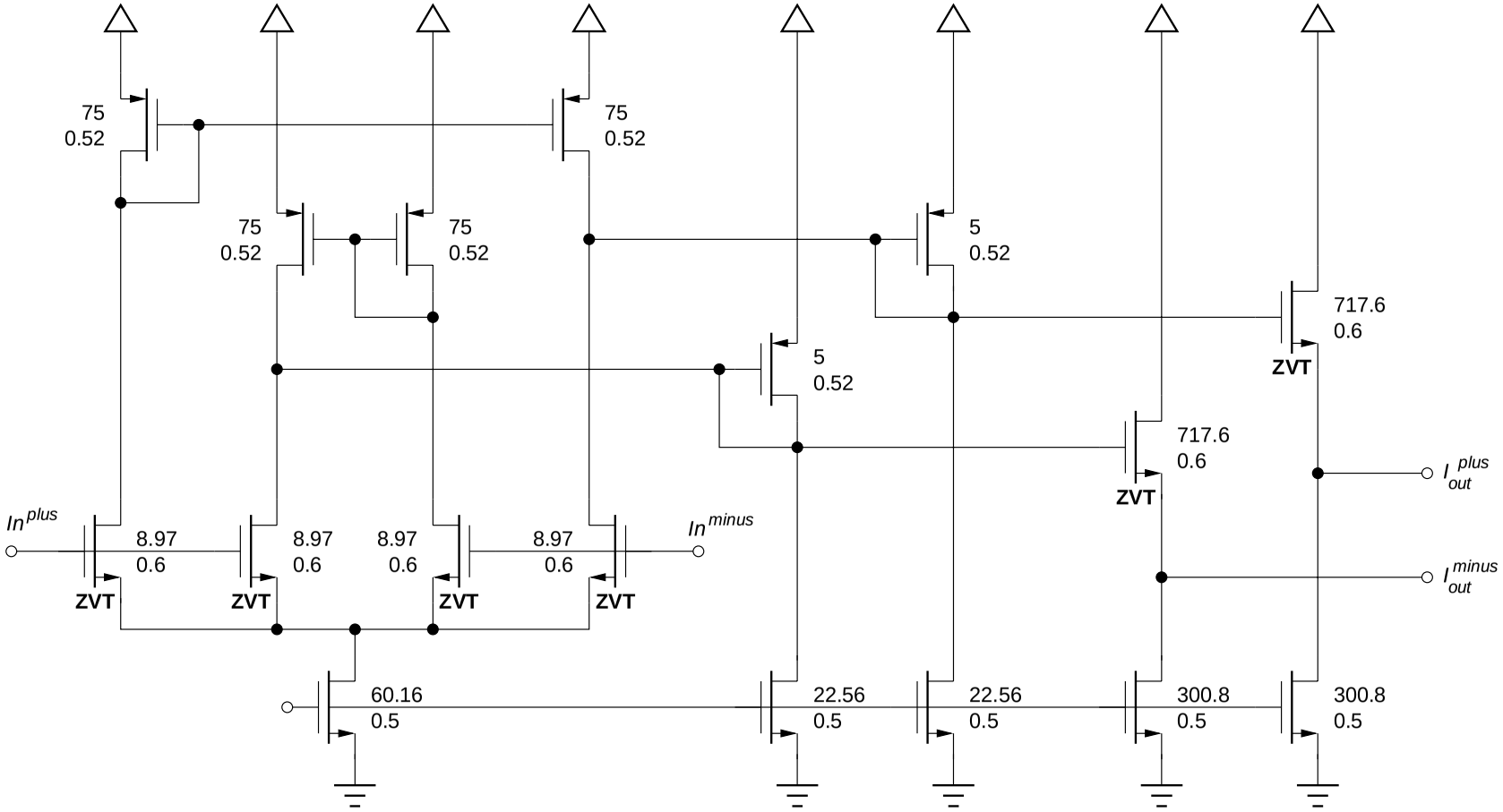
Current output driver



fully differential transconductance amplifier

- In(plus): output of multiplexer source follower
- In(minus): output of the dummy channel

common mode subtraction

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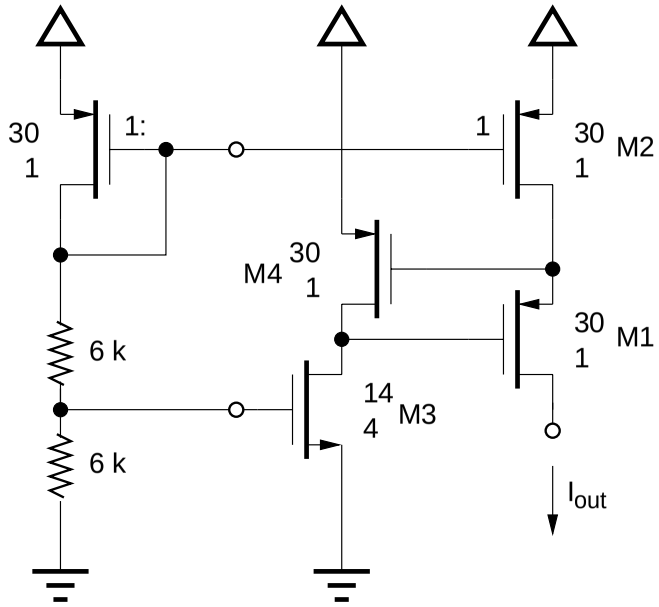
Current source



- cascode is formed by M1 and M2
- feedback loop (M1, M4 and M3) stabilises the drain−source voltage of M2

Implemented as a regulated cascode configuration

- nominal output 126uA

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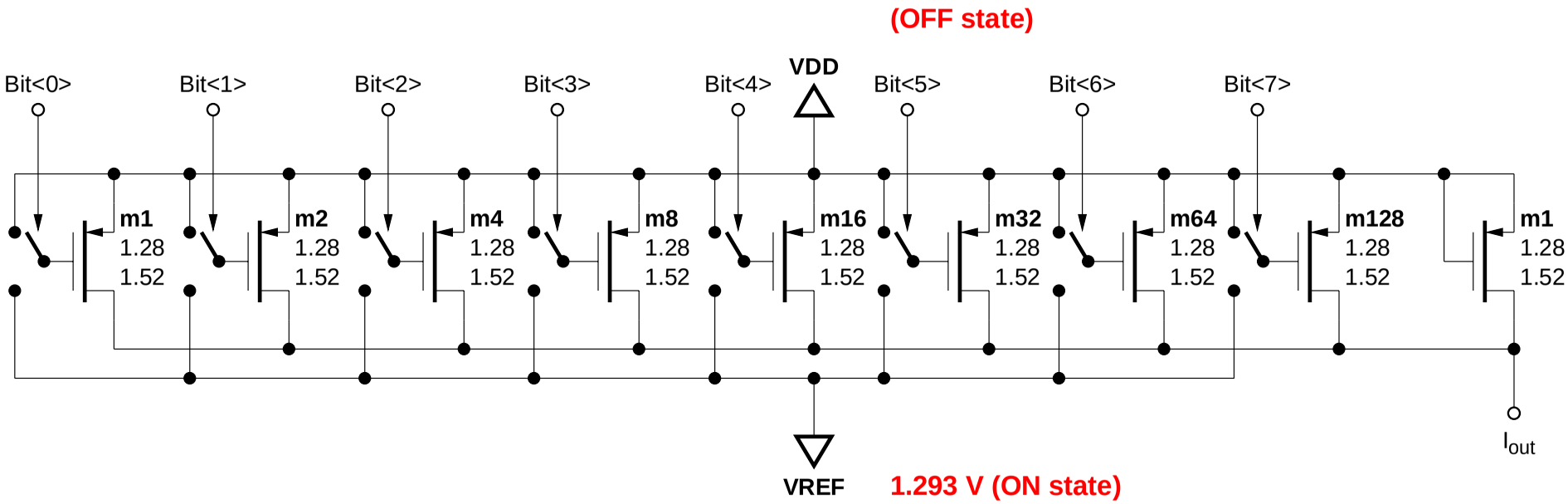
Current DAC



− binary−weighted current sources

− PMOS transistors are arranged in a "common centroid" layout configuration
homogeneous structure guarantees a good matching

− maximum output current: 2.03 mA

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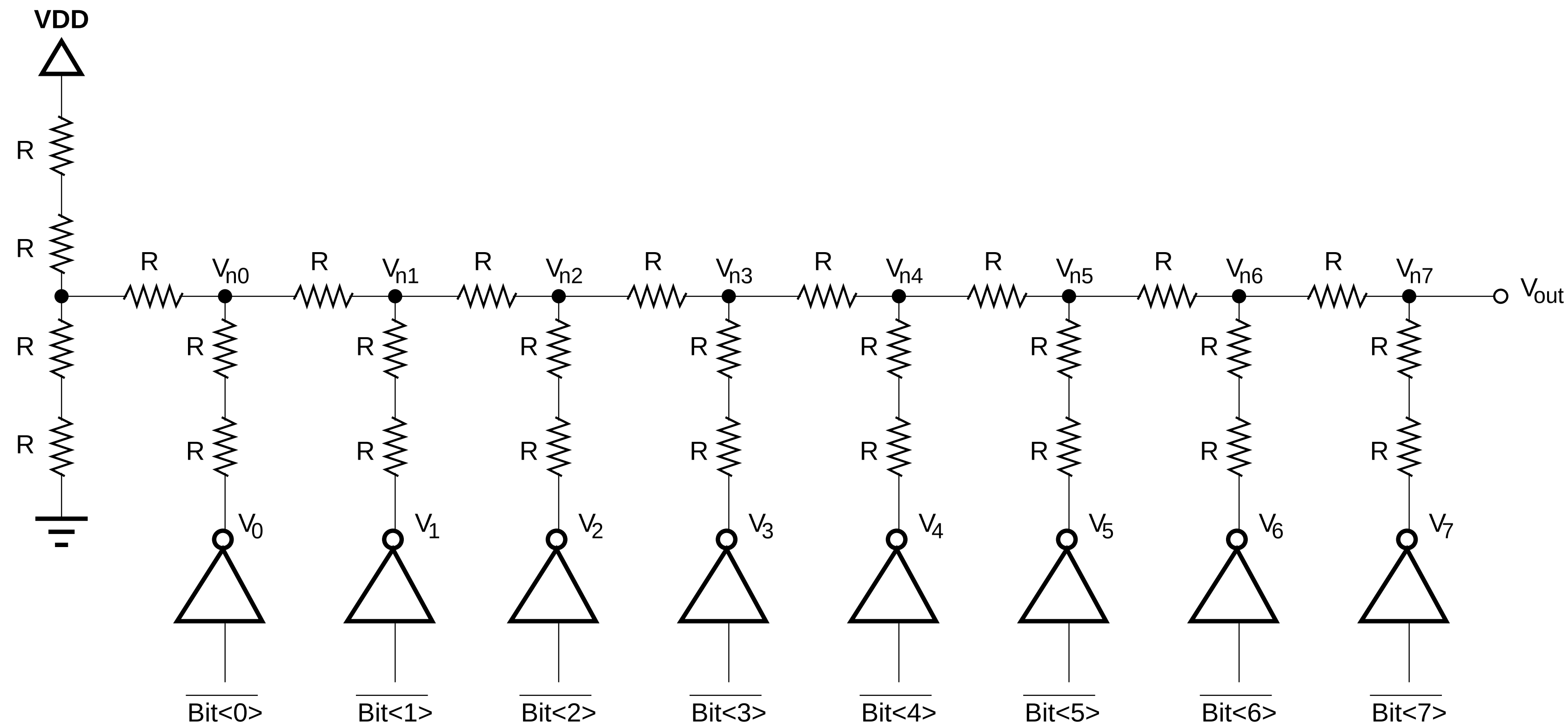
Voltage DAC



- R−2R ladder configuration
- resistors are made of non−silicided polysilicon

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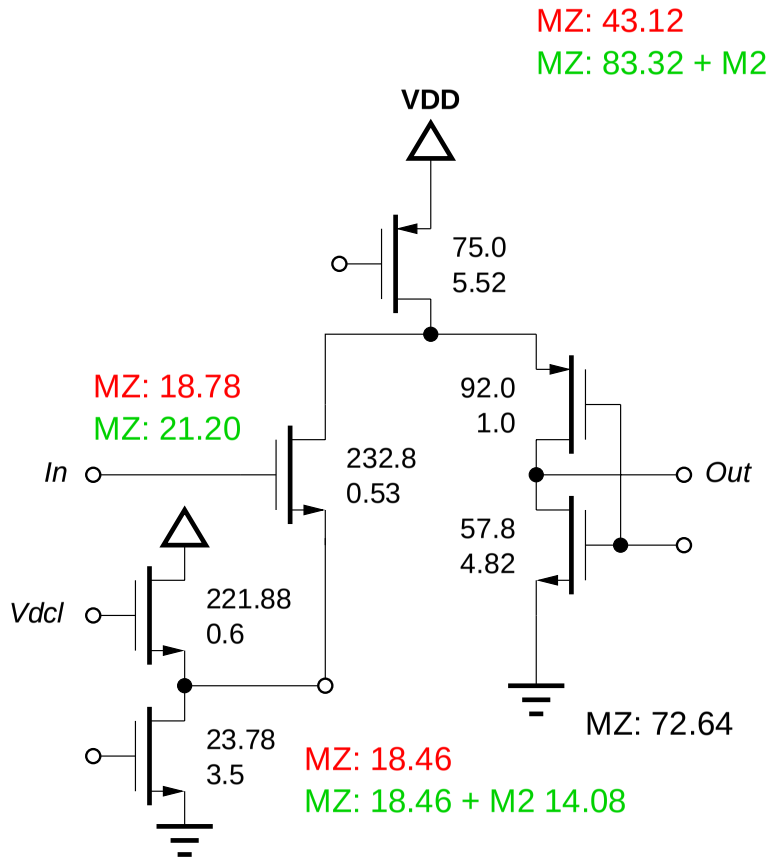
Power routing (Pipeamp)

Power routing



red: power routing on Beetle 1.2

green: power routing on Beetle 1.2 MA0 (RICH) and next version 1.3

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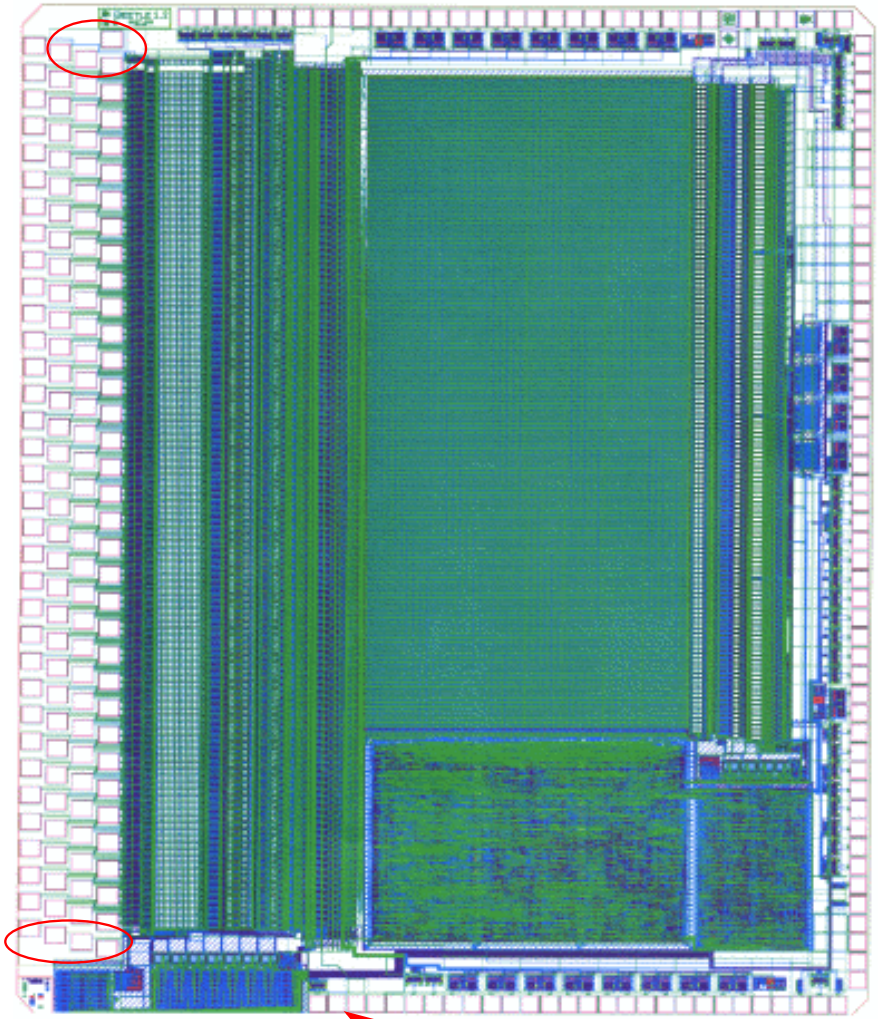
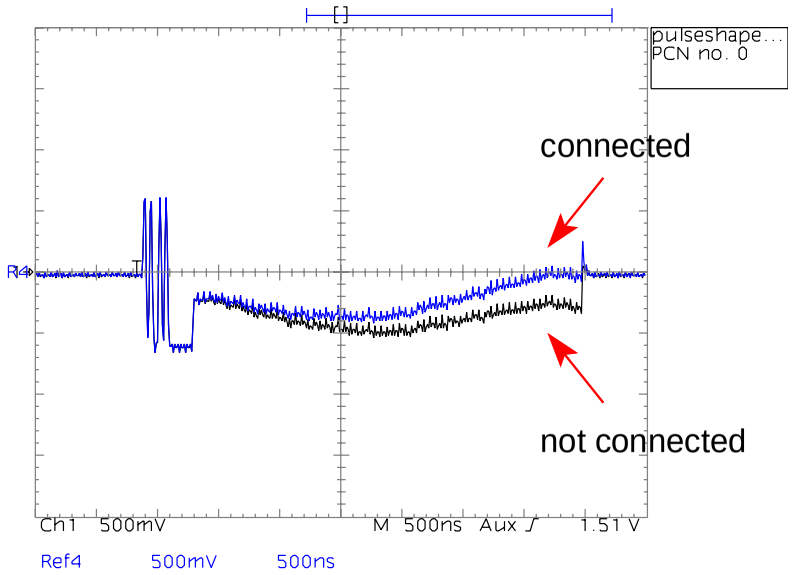
Power routing (Front−end)



this vdda−pad is on Beetle 1.2 connected to the front−end power



Beetle 1.2 readout with:

− pad connected to vdda

− pad not connected to vdda (comparable to Beetle 1.1)

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