Architecture and Concepts

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Beetle: Application and Requirements

LHC Accelerator:
- 40MHz BX clock

LHC*b* Experiment:
- 4μs = 160 BX clock cycles L0 latency
- max. 16 (consecutive) pending triggers
- Readout time: 900ns/trigger
- Fixed length of data frames
- TTC/DCS compatible control signals

Vertex Detector (VeLo):
(Silicon Strip Detector)
- 10Mrad TID radiation hardness
- ≤25ns peaking time
- ≤6mW/ch power dissipation
- ≤30% signal remainder from preceeding BX

Pile-Up Veto counters (Veto):
(Silicon Strip Detector)
- Same as Velo plus
- prompt binary readout with reduced granularity
- global and per-channel threshold adjustment
- discriminator channles maskable

Silicon Tracker (ST):
(Silicon Strip Detector)
- Similar to Velo plus
- compatible with >30pf strip capacitance
- Driving capability ≥10m TP cable

Ring Image Cherekhov detector (RICH):
(Multi-anode PMTs)
- Different Front End
- binary pipelined readout
- 80MHz readout clock

Beetle = "HELIX" (RD20 + prompt discriminators) architecture + pipelined binary mode

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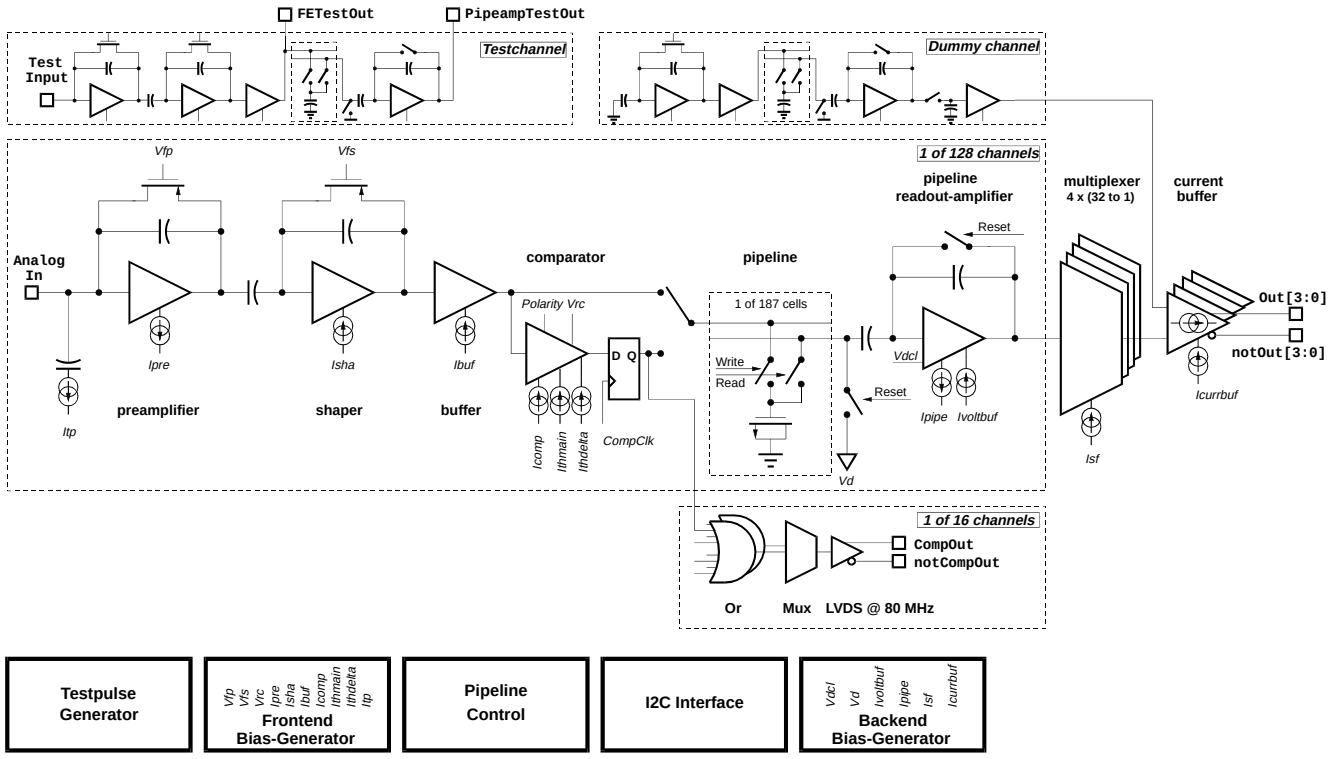
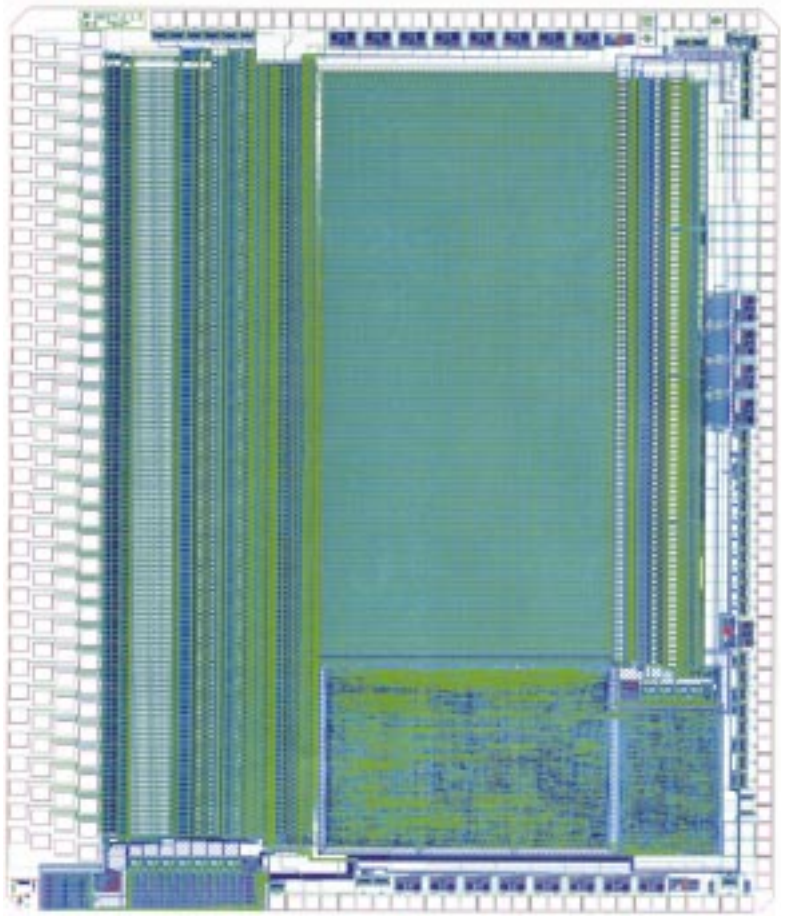
Beetle: Block Schematics (I)

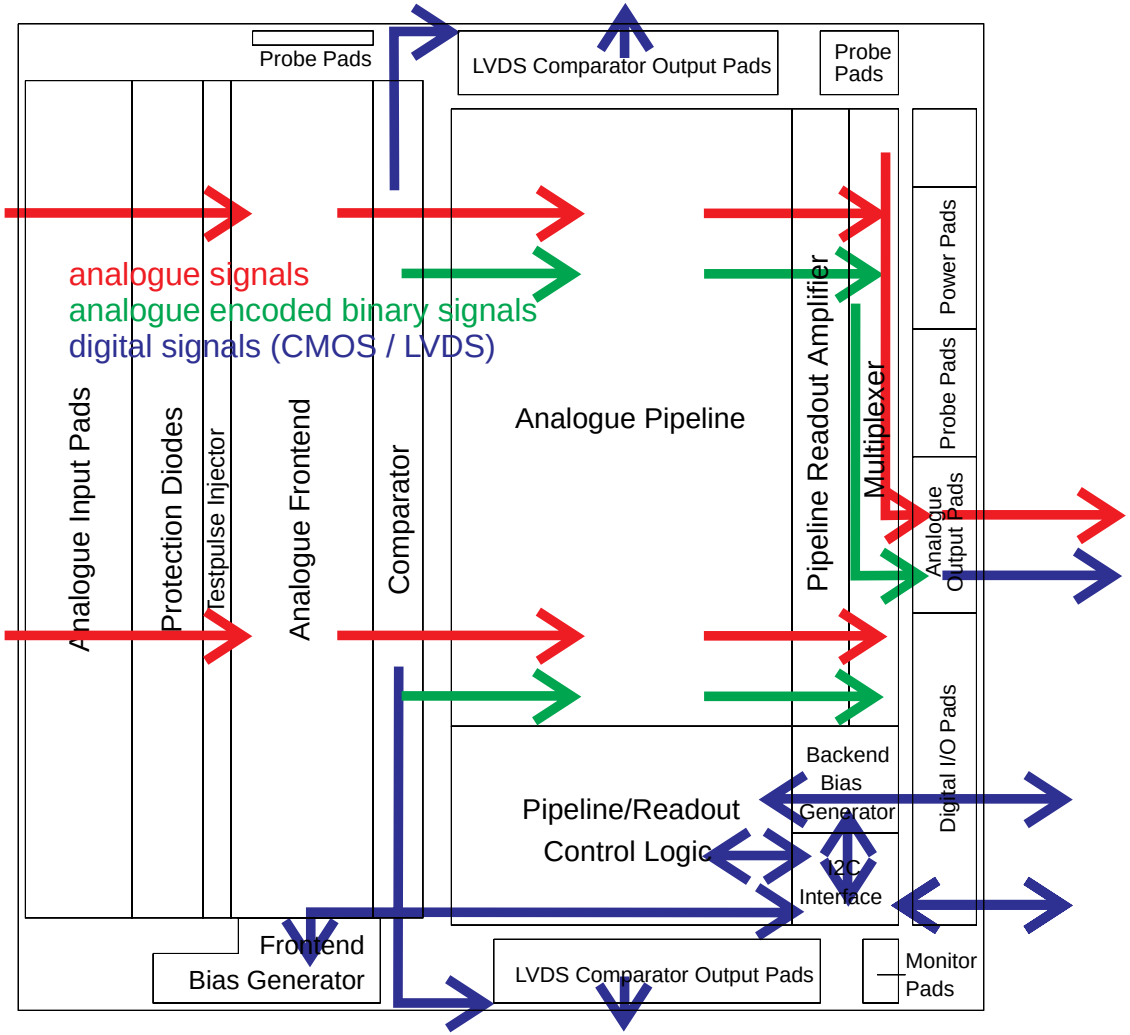


Features:

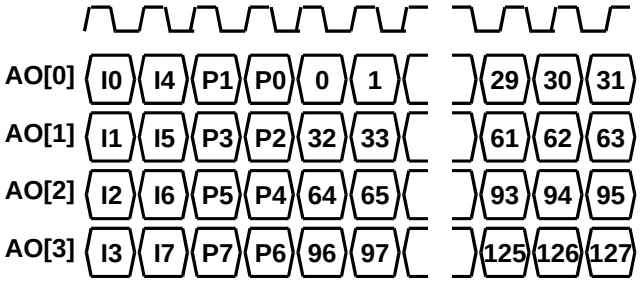
- 128 input channels
- CSA/Shaper with 25ns peaking time
- 40 MHz sampling (LHC clock)
- 128 discriminators with switchable polarity
- analogue memory for 160 sampling steps
- buffer for 16 triggered events
- ➔ 4 µs max. latency
- ➔ 900ns/event readout speed
- internal DACs for bias settings
- test pulse injector with adjustable amplitude
- setup/slow control via I^2C interface

Beetle: Block Schematics (II)

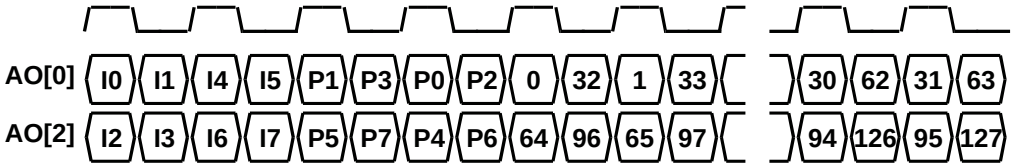




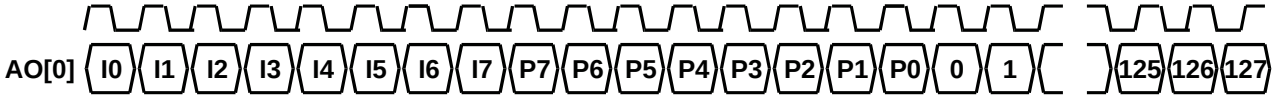
Beetle: Readout Modes



VeLo/ST



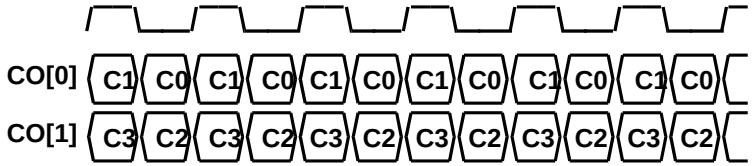
RICH



Lab

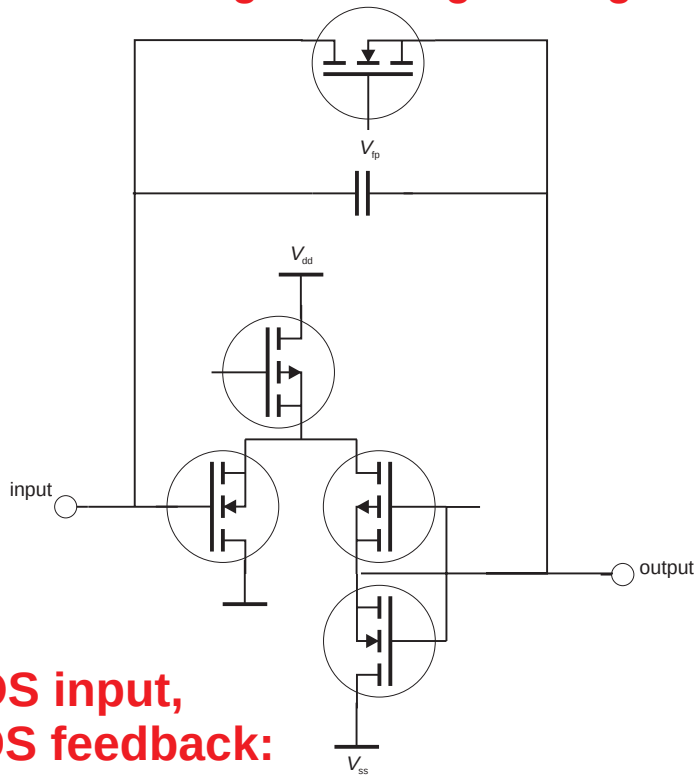
Bit	Description
I0	Start Bit: Always 1
I1	(even) parity of pipeline column number (PCN)
I2	ActiveEDC: indicates active error correction logic (EDC)
I3	parity of *CompChTh* register
I4	parity of *CompMask* register
I5	parity of *TPSelect* register
I6-I7	2 LSB of *SEUcounter* register
P0-P7	Pipeline column number (PCN)

Comparator
(Veto counters, prompt binary readout)



Beetle: Amplifier Stages

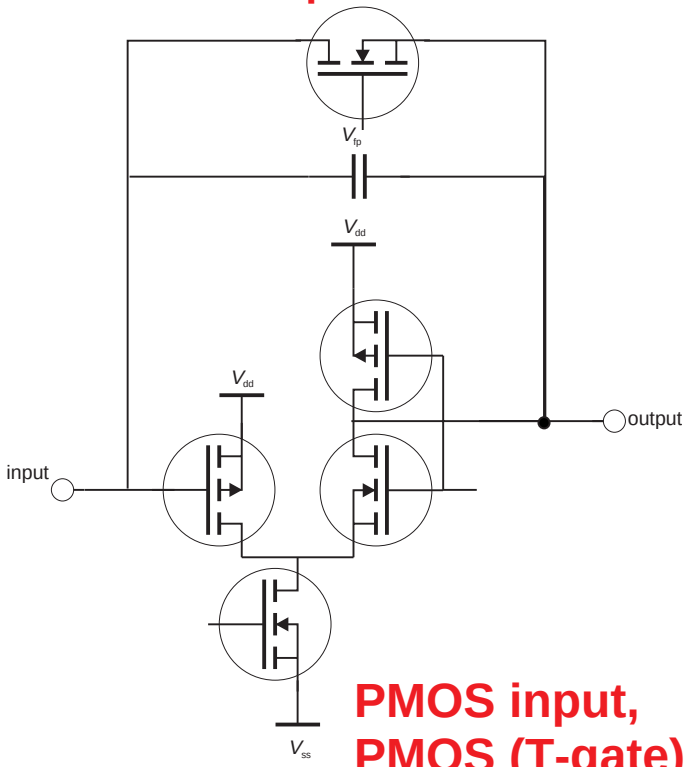
all single-ended gain stages are folded cascode amplifiers



NMOS input,
PMOS feedback:

- high g_m/area of input transistor
- feedback control voltage limited by power supply rail

Preamp, pipeline readout amplifier



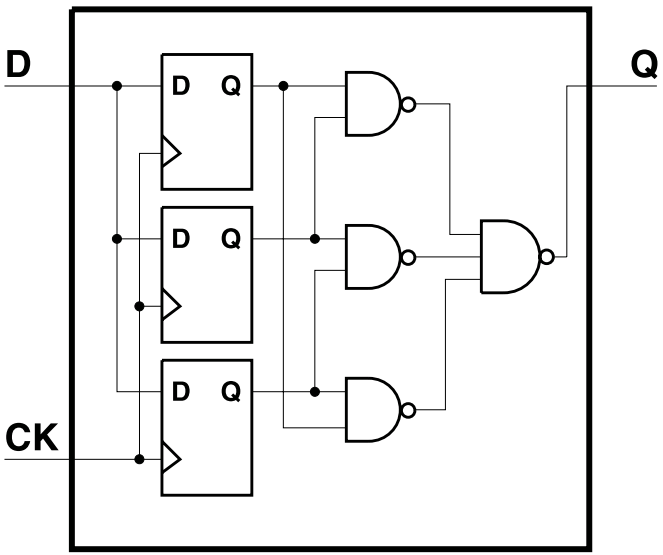
PMOS input,
PMOS (T-gate) feedback:

- no limitations for feedback transistor design
- low g_m/area of input transistor

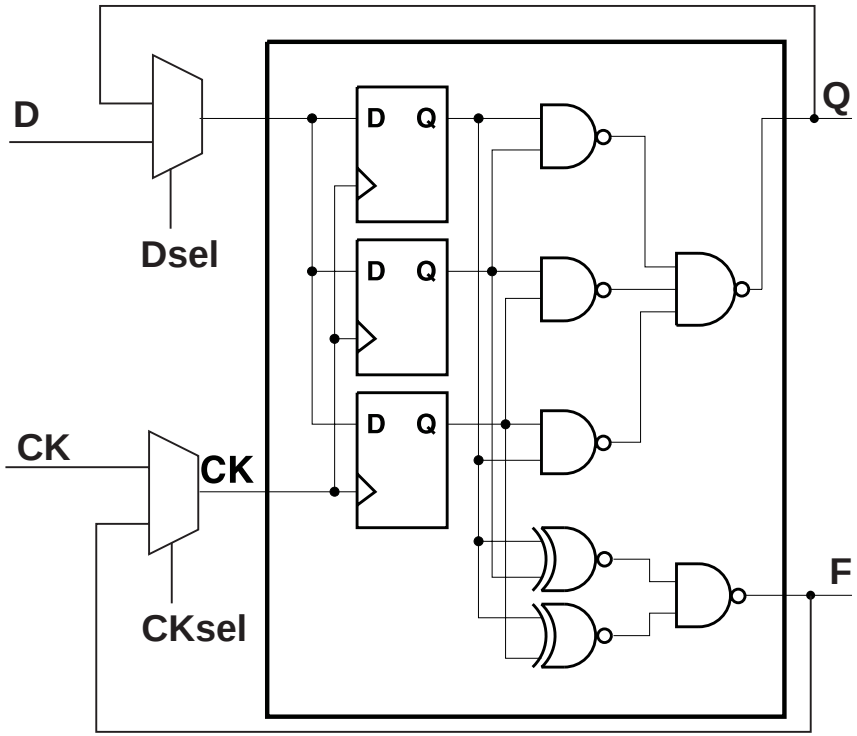
Shaper

Beetle: SEU Robust Circuits

State machines



Static registers



Beetle: Other Features

10Mrad radiation hardness:
- commercial 0.25µm CMOS technology
- enclosed gate structures (for all NMOS FETs)

SEE protection:
- guard rings and substrate contacts to prevent SEE
- triple-redundant registers (with autocorrection)

Adjustable pulse shape:
- adjustable preamp and shaper feedback (I^2C)
- adjustable bias currents (I^2C)
- on a per-chip basis to match different detector characteristics

Test pulse:
- adjustable charge injection (I^2C)
- switchable polarity
- channel mask (I^2C)

Output drivers (pipelined mode):
- fully differential current drivers (analog mode)
- can drive 10m of TP cable
- LVDS levels in binary mode

Binary readout (fast comparators):
- global (8bit) and per channel (3bit) threshold adjustment (I^2C)
- adjustable high-pass filter for common-mode supression (I^2C)
- channel mask to supress noisy channels
- switchable polarity