Digital Functionality of the Beetle Chip

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Outline

Hierarchy levels

I2C Interface

SEU Robustness

Pipeline/Readout Control

Readout Sequence

"Sticky Charge" Effect

Intended Digital Changes in Beetle1.3

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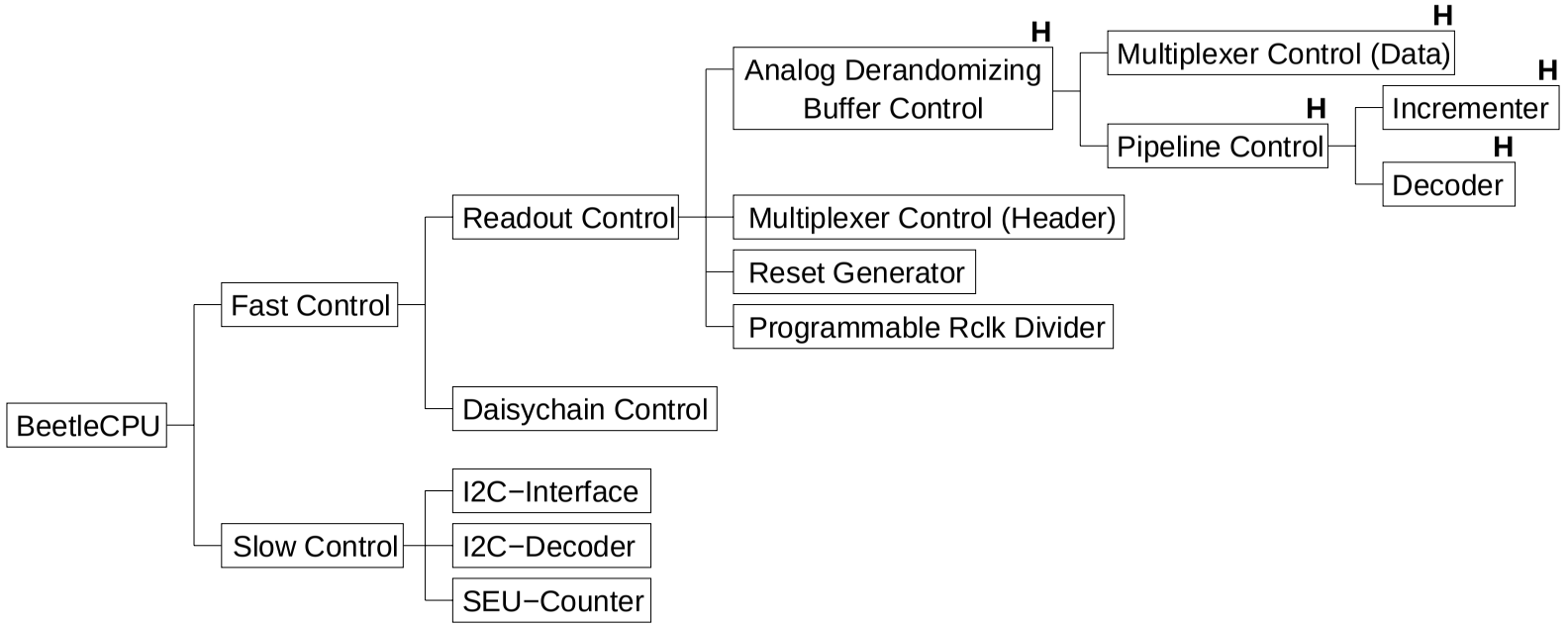
Hierarchy Levels



Functional description in Verilog

Synthesis: Synopsys

Place & Route: Silicon Ensemble

Fast Control and Slow Conrol also separated in Layout (different clock domain)

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I2C Interface

Registers

16 bias registers (8 bit): Vfp, Vfs, Ipre, ...

4 configuration registers (8 bit): Latency, ROCtrl, RclkDiv, CompCtrl

1 register: SEU counter (8 bit)

1 shift register (384 bit): CompChTh

2 shift registers (128 bit): CompMask, TpSelect

since version Beetle1.2: SCHMITT triggers in pads

planned: 5 V compatible pads

no external level shifting devices

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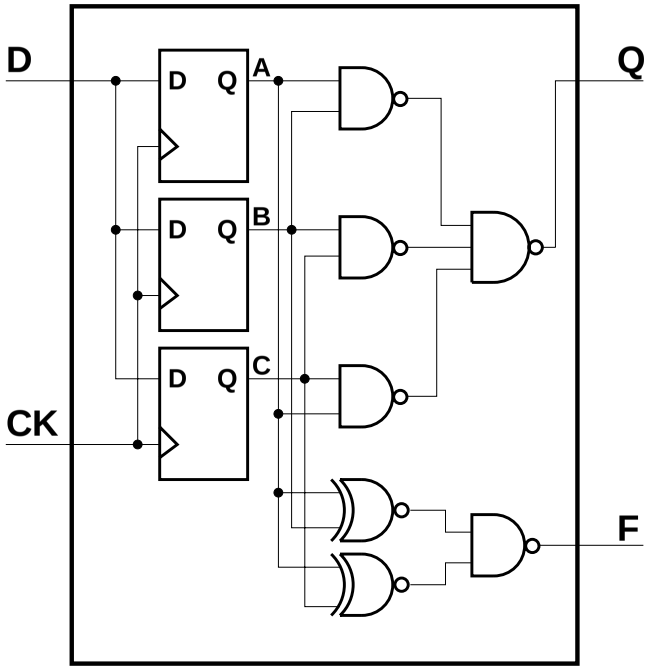
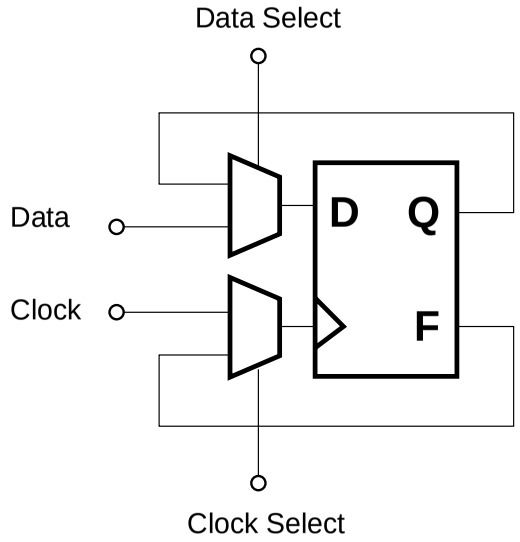
SEU Robustness: self−triggered correction

FSM state registers + flip−flops in logic: triple redundant

Beetle registers (bias, configuration, ...): red. + self−triggered correction





no. of corrections is counted! (SEU counter)

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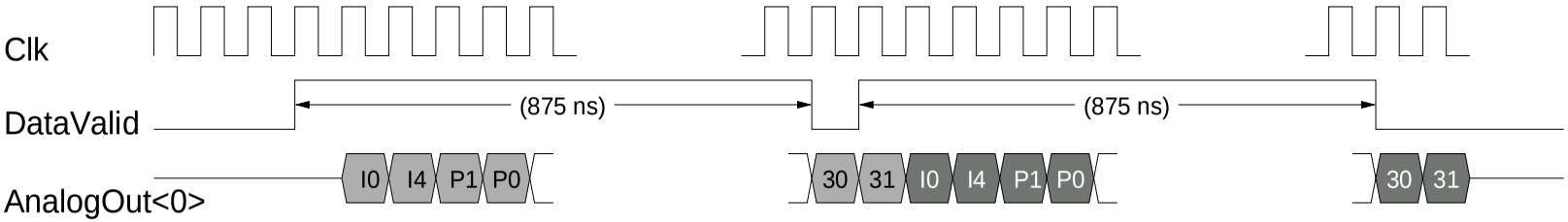
Readout Sequence

Timing

Consecutive Readout



Header

16 bits: I0: leading bit: always 1

I1: (even) parity of pipeline column number

I2: ActiveEDC: indicates active EDC logic

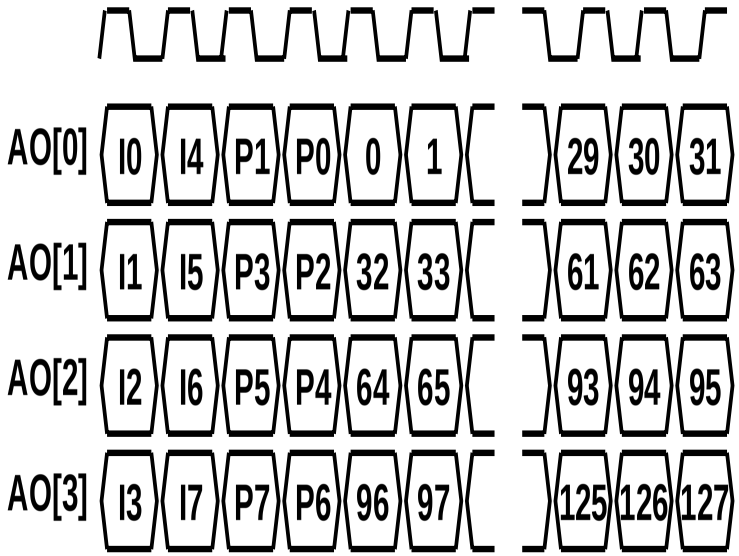
I3: parity of register CompChTh

I4: parity of register CompMask

I5: parity of register TpSelect

I6−7: 2 LSBs of register SEUcounter

P0−7: pipeline column number



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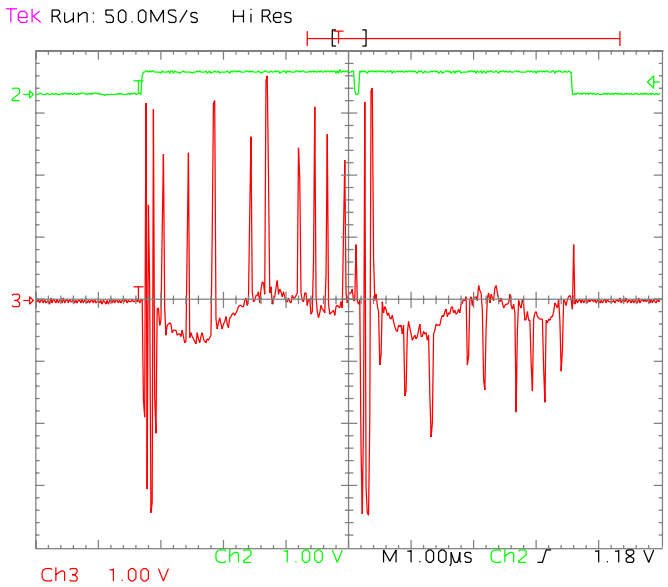
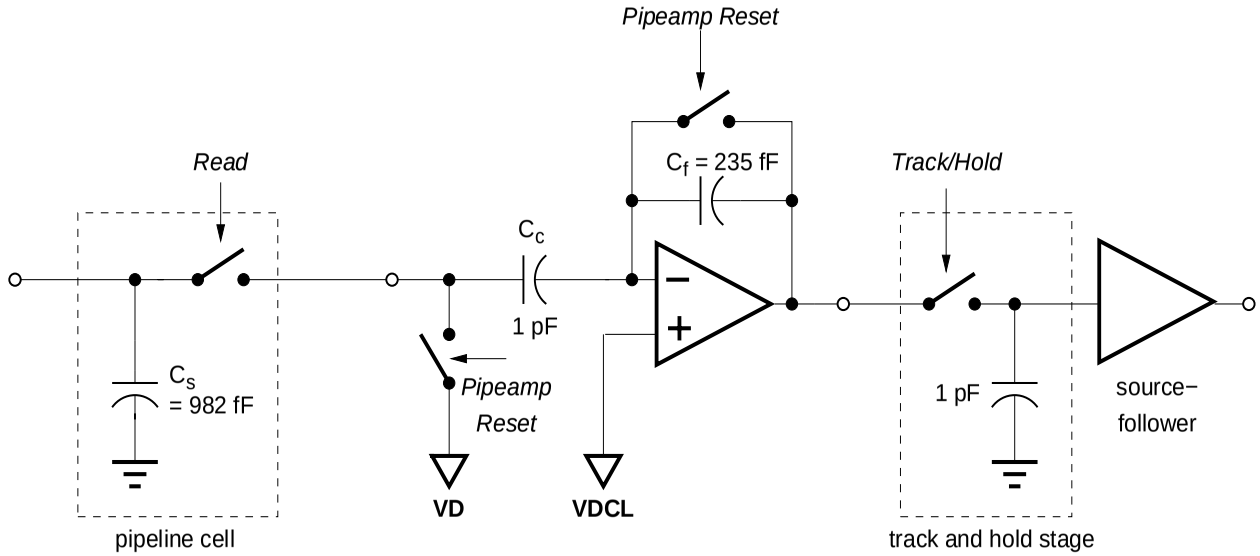
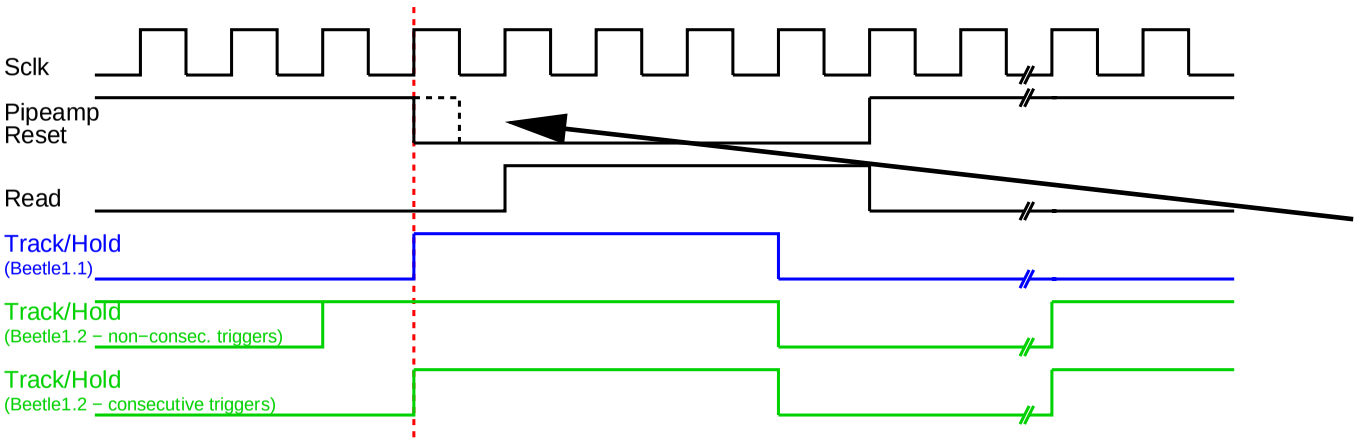
"Sticky Charge" Effect







Modification in Beetle1.3

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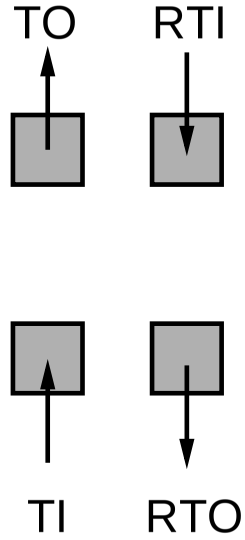
Intended Digital Changes in Beetle1.3

I2C Pads

Daisychain Control

- DaisyLast is sensitive to RTI: add switch
- add state in FSM for f(Rclk) < 0.5 f(Sclk)



Timing scheme Pipeamp (sticky charge effect)

- shift PipeampReset by 12.5 ns

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