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DRAFT

The VELO F/E-Chip

This document is an attempt to collect the criteria which are relevant for the F/E-chip of the LHCb VErtex LOcator (VELO). The specifications given below are the result of extensive discussions. Nevertheless, some numbers still have to be verified or confirmed within the VELO-group.

status: working document

1 Introduction

The successful operation of the LHCb experiment depends critically on the performance of its vertex detector, the VELO (VErtex-LOcator). A crucial element of the system is the front-end chip. This document collects criteria which are relevant to assure that the chip works within LHCb such that the physics performance is not compromised.

In section 2 first the operating environment of the chip is defined. Then the boundary conditions are given in section 3, which the chip has to satisfy. In section 4 the measurements are defined which are needed as input for a determination of the physics performance; a proposal is made how to quantify this is given in section 5. After that, system tests are discussed in section 6 and the acceptance criteria defining a good chip in 7. Definitions of procedures and results from actual measurements are collected in the appendix.

2 Operating environment

The operating environment for the VELO frontend chip is summarized by tab. (1).

environment		
1.1	total radiation dose	10 Mrad
1.2	average dose rate	0.2 rad/s
1.3	max. capacitive load	30 pF
1.4	max. load variation/chip	10 pF (?)
1.5	max. occupancy	5 %
1.6	temperature range	-30 to $+60$ C

Table 1: Operating environment of the VELO frontend chip

The number for total dose and dose rate are based on estimates of the particle flux at the location of the F/E-chips, and the requirement that the chip should be allow 5 years of operation, assuming 10^7 seconds of running per year. The 10 Mrad figure comes from a

simulation [1] which indicates a total dose at the location of the chips of 0.16-0.32 Mrad/year, a total running time of 5 years, and safety factors of 2 each for the accuracy of the simulation, the qualification procedure and component variations in the chip. The capacitive load and load variation over a single chip are determined by the properties of the sensors and still may change. The current results are based on measurements of the noise variations across a sensor [2, 3] for existing prototypes. The occupancy follows from sensor geometry and particle flux. The average occupancy for B-events is only 1%. The 5% figure given above is chosen to make sure that the detector can also cope with bursts of events and to have some safety margin for high luminosity running. The temperature range finally reflects the full range expected from operation of the system with and without cooling.

3 Basic specifications for the frontend chip

The F/E-chip has to fit into the general LHCb DAQ- and ECS-infrastructure and thus has to fulfill a certain number of mandatory requirements in order to be operable in the experiment. These are listed in tab. (2).

	DAQ requirements		Beetle 1.2
2.1	sampling frequency	40 MHz	OK
2.2	max. L0 latency	4 μs	OK
2.3	L0 accept rate	1 MHz	OK
2.4	consecutive triggers	yes	OK
2.5	multi-event buffer	16	OK
2.6	max. readout time	900 ns	OK
2.7	registers read-back to ECS	yes	OK
2.8	fast reset of pipeline and fifo	yes	OK
2.9	differential inputs for trigger and clock	yes	OK

Table 2: Mandatory requirements to the VELO frontend chip

If any of the above points is not met, then the chip cannot be used. In addition there are performance requirements which are specific for the VELO and which, within certain limits, have to be considered as soft boundaries. If all requirements listed in tab. (3) are satisfied, then a satisfactory performance of the VELO can be expected, which allows to reach the LHCb physics goals. Deviations from the target numbers given in tab. (3) may be acceptable, if compensated elsewhere. This issue will be addressed in section(5).

The maximum allowed power consumption/channel is given by the dimensioning of the cooling system of the VELO. Here all the power has to be counted which is dispersed in the vacuum of the VELO vessel, i.e. the chip plus output driver stages. Peaking time and pulse spill over reflect the requirements of the L1 trigger of fast signal sampling in the VELO with little remainder from the previous bunch crossing. The dynamic range and the non-linearity together with the ENC and cross-talk numbers determine the accuracy and efficiency of a coordinate measurement.

The dynamic range quoted in tab. (3) corresponds to ± 5 MIPs of 22 ke, which should be large enough to handle most of the charged particles traversing the detector. The non-linearity

	basic VELO requirements		Beetle 1.2
3.1	max. total power consuption/channel	6 mW	OK
3.2	max. peaking time	25 ns	OK
3.3	max. pulse spill over after 25 ns	30 %	OK
3.4	max. non-linearity over $\pm 110,000$ e^-	5%	OK
3.5	max. cross talk between channels	5%	OK
3.6	max. total ENC at 10 pF capacitive load	1500 e^-	OK
3.7	min. tolerable input current	20 nA	OK
3.8	min. output driving strength at 100 Ohm TP	1 m	OK
3.9	min. chip yield	30%	OK
3.10	synchronization check with PCN	yes	OK

Table 3: Target specifications of the VELO frontend chip

and the cross talk figure are based on a simulation result [4], which indicates that there is only negligible performance degradation as long as the precision of the digitization is done with at least 4 bits, or 6.25% non-linearity over the dynamic range of the signal. The ENC number is such, that a 22 ke MIP will be measured with a S/N=14. This gives a comfortable margin for safe operation of the VELO, since the hit finding efficiency is found to be stable down to values S/N=10 [5]. Note that the *total ENC* covers not only the noise contribution from the frontend, but also the contribution from the pedestal fluctuations along the pipeline.

The tolerable input current into the F/E quoted above is derived from the requirement that a charge of 50,000 electrons is sampled at a rate of 2 MHz. The required driving capability is determined by the location of L1-buffer on the detectore. The required chip yield, finally, is driven by the condition to be able to buy all chips needed for the VELO with one production run.

In order to be able to monitor the correct operation of the chip at least the synchronization check via pipeline column number is required. Additional SEU robustness and monitoring features may be desirable.

4 Single chip measurements

The list of required measurements given in tab. (4) is a compilation of single chip measurements that can be done under laboratory conditions. The items allow to gauge the single chip performance and will be the basis to extrapolate to the ideal performance that can be expected in the experiment. The measurement should be done for unirradiated chips and chips irradiated to 10 Mrad, in order to see how much performance degradation can be expected during the lifetime of the sensors. If only one of the two conditions can be tested, then measurements with irradiated chips should have priority, to get at least a lower bound for the expected chip performance.

1. random trigger test
    - 40 MHz sampling clock
    - 1.1 MHz random trigger
    - minimum 48 hours continuous running
2. overclocking test
3. random trigger test
    - maximum frequency of operation for the digital part
    - evolution of analog front-end characteristics
4. pulse shape characteristics after 1m Twisted Pair with 100 Ω
5. saturation
    - maximum rate of 22 ke Pulse
    - maximum charge at low rates (1 Hz)
    - response to heavy ionizing particles, charge > 120 ke
    - saturation (gain degradation) as function of input charge
6. range of reliable power supply operation
7. pipeline and channel homogeneity
    - rms pedestal along the pipeline
    - rms pedestal over all channels (integrated over the pipeline)
8. total power consumtion of the chip when clocked and triggered
    - at minimal settings (powered but not operated)
    - at nominal settings
    - at maximal settings
9. demonstrate operation at -30C and $+60$C
10. ENC vs $C_{\texttt{load}}$ at room temperature
    - using test charge injection
    - corrected for gain variations
11. pulse shape characteristics
    - peaking time
    - rise time
    - remainder after 25 ns
    - maximum undershoot
    - remainders after $n \cdot 25$ ns

Table 4: Lab measurements for the VELO frontend chip

5 Interpretation of results

Given the information from the lab measurements, it remains to gauge the performance in the experiment. The proposal is to estimate

- the fraction of hits lost
- the fraction of hits which are spillover from a previous event

These quantities can be determined from knowing the distribution of the charge deposited in a sensor, the distribution of the load capacitance and the occupancy. The charge deposit distribution has to be given for minimum bias events and for triggered events. It should be extracted from a full simulation. For the chip one needs to know the pulse shape as function of the input charge as well as ENC and gain as function of the load capacitance. Concerning the pulse shape, it would be best to have it at sampling points $n \cdot 25$ ns after the peak, with $n = 0, 1, \ldots, 5$.

In addition it would be desirable to have an estimate of the SEU rate for the frontend chip, either from direct measurements or calculations based on existing SEU cross sections and the simulated LHCb particle fluxes. These figures then should be converted into expected inefficiencies for LHCb physics running.

6 System tests

Given the single chip measurements and an interpretation of the results in terms of physics performance, this interpretation has to be cross checked against system tests based on fully equipped hybrids attached to silicon sensors. The most important quantities determined by these system tests are summarized in tab. (5).

1. pulse shape characteristics
2. peak S/N values for beam related hits
3. common mode noise for the chips
4. power supply rejection
5. hit finding efficiencies
6. fraction of noise hits vs efficiency

Table 5: Quantities to be determined by complete system tests

The determination of the pulse shape characetristics just checks that the lab measurements map correctly to the final operating environment. The S/N can be compared directly with the expectations according to section 5. Common mode variation due to external pickup or power supply variations reduce the dynamic range of the chip and thus should be limited to something on the order of a MIP signal. If it is so large that there is danger of compromising the physics performance, then a detailed study would be needed to find out whether the problems are intrinsic to the chip or to some design feature of the hybrid.

7 Acceptance criteria

Here a proposal is made to define the acceptance criteria for the VELO frontend chip and a procedure to verify that the yield is sufficiently large.

Chips to be installed in the VELO detector should be tested on a heated wafer prober, in order to deselect candidates that may work while still cool but then fail during operation. The test procedure has to cover digital and analog performance of the chip.

The digital test should consist of

- programming and read-back of all registers, and
- running a well defined trigger sequence

This test must be passed without error. It should be run with a clock frequency of at least 40 MHz, possibly even higher. The analog test should cover a

- rough check of the ENC for all channels and a
- full pipeline scan.

A chip fails the analog test when one dead channel or one dead pipeline column is detected, or when the total ENC for one channel exceeds 2500 e^-. These criteria are chosen such, that a single chip is guarantied to be more than 99% efficient.

References

[1] particle flux simulations by Ivan, Gloria ???

[2] Thesis Stefania Saladino

[3] Paula Collins, presentation at the Chip meeting September 30

[4] Hans Dijkstra, pivate communication

[5] Silicon Tracker TDR

Appendix

A Definition of procedures

Here the procedures are defined which are used to determine the quantities that were measured.

A.1 Yield determination

Given a test procedure for individual chips, the existence of a minimal yield is established by the following procedure. Chip tests are performed until 20 good ones have been found. Assuming binomial statistics and a true yield of 30%, one finds that in 99% of all cases the required number has been found after having tested 100 chips. Turning the argument around, one can define that the yield is insufficient if a sample of 20 good chips has not been found after 100 tests.