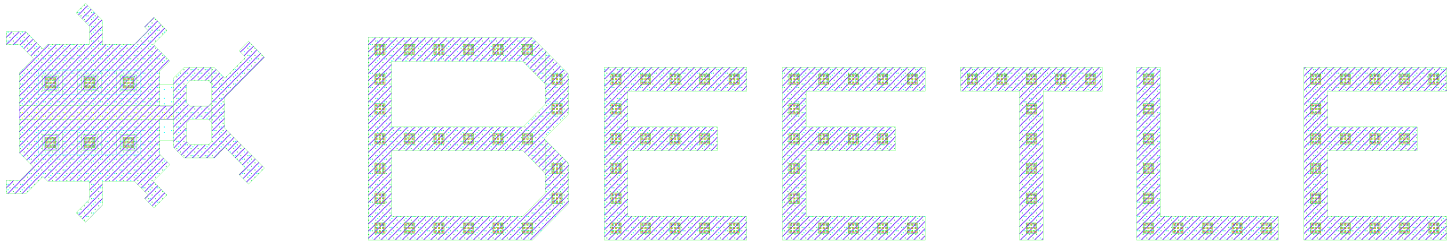

- Project Overview -

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Beetle: A Readout Chip for LHCb

- analog/binary pipeline chip
- providing a prompt binary readout for trigger applications
- integrated in a standard 0.25µm CMOS technology
- designed for:
  - Silicon Vertex Detector
  - Pile-up Veto Trigger
  - Inner Tracker
  - Rich (in case of MAPMTs)

Key Specifications:

- 40MHz sampling
- Max. latency 4µs
- 40/80MHz readout
- Fast shaping:
  - $t_{rise} \leq 25$ns
  - remainder 25ns after the peak ≤30%
- accept up to 16 (consecutive) tiggers
- Readout time ≤900ns/trigger
- Rad hard ≥10Mrad

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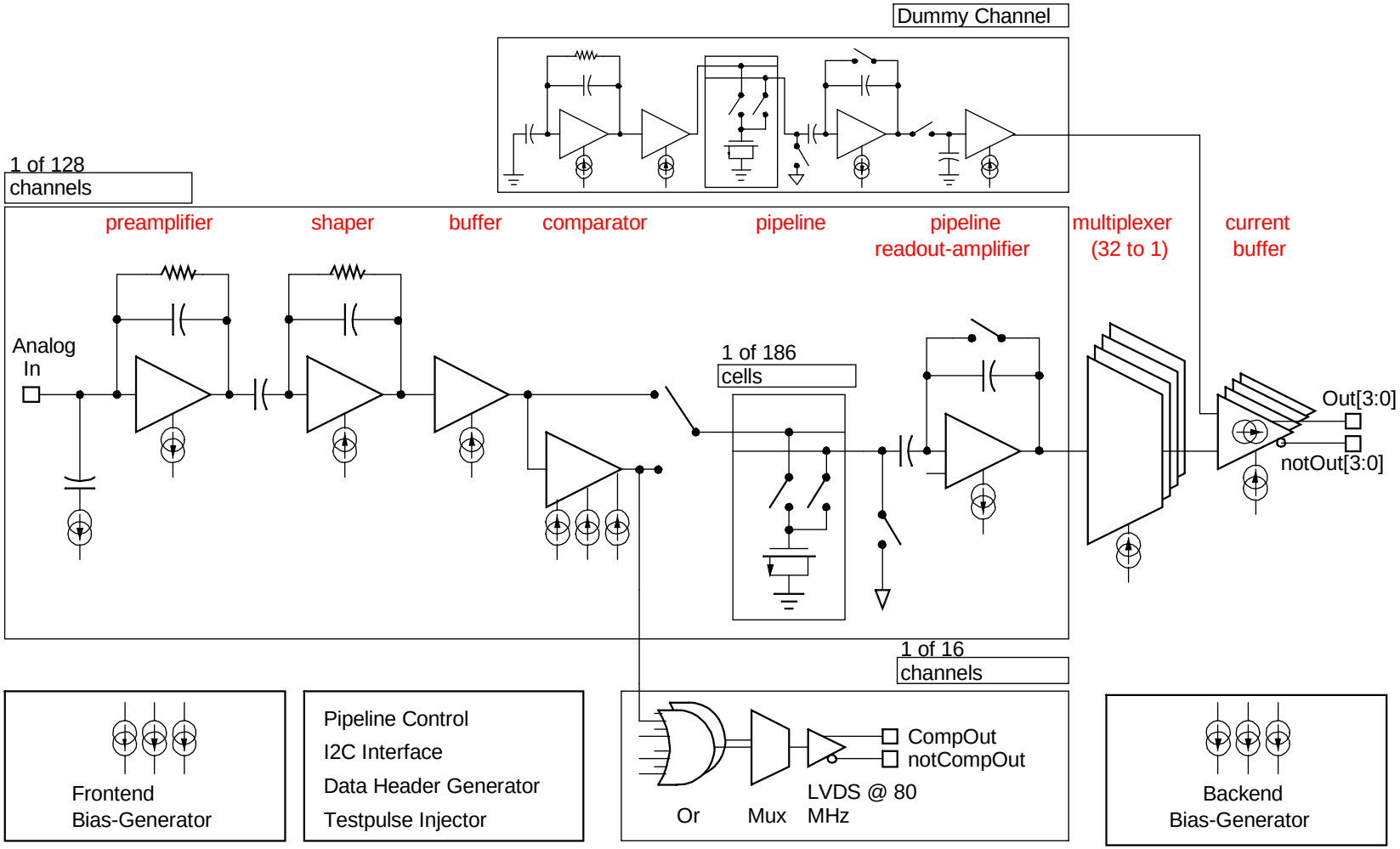
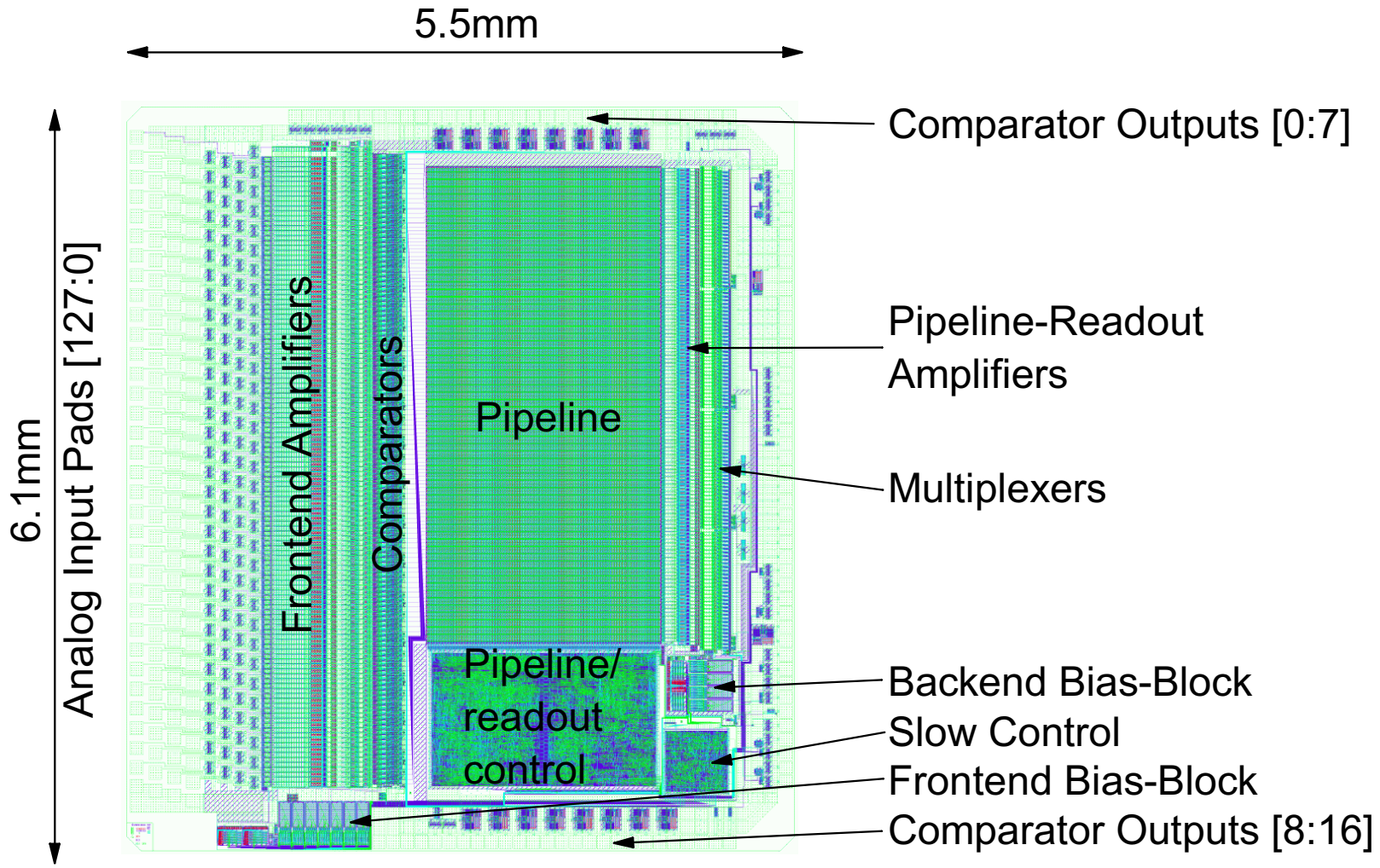
Beetle: Block Schematics



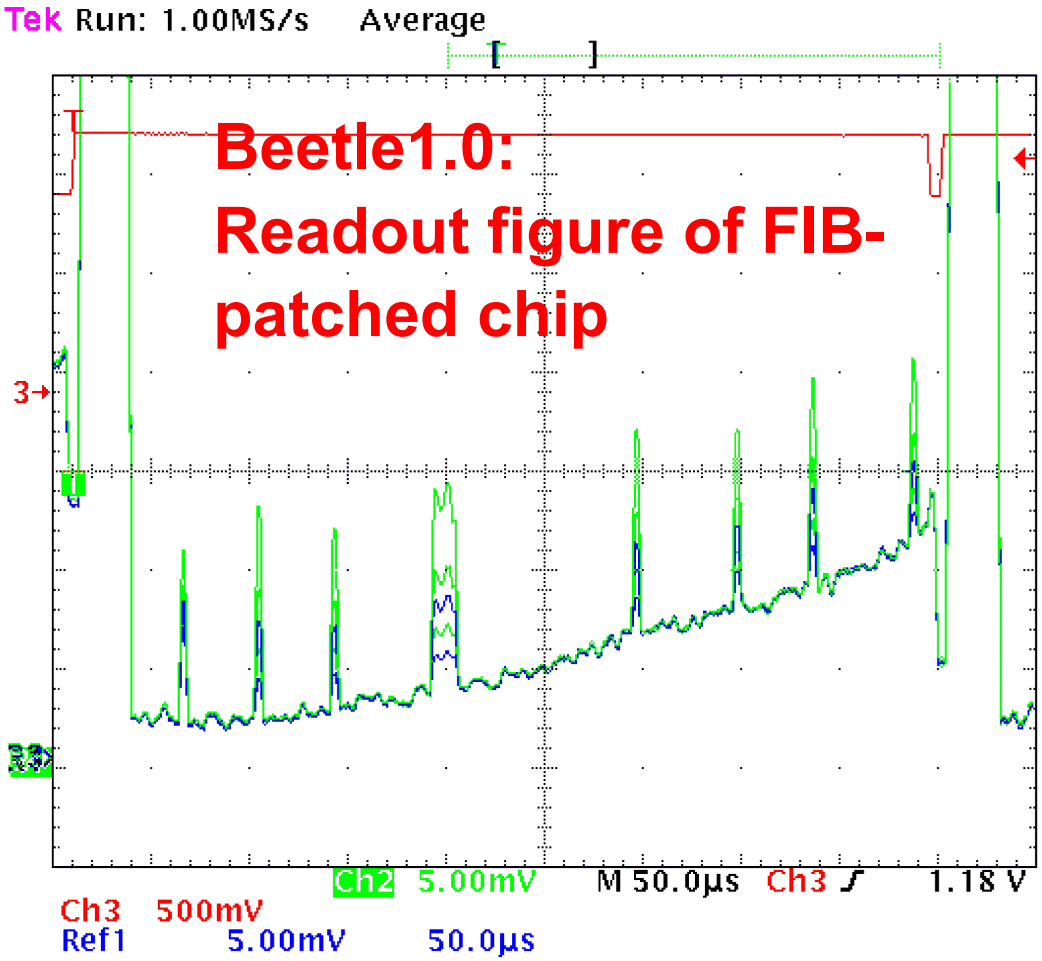
Beetle: Layout/Floorplan



Beetle: Other Features

- Slow Control via standard I2C interface (7bit address mode)
- Self-programming address assignment @ powerup
- Readable setup registers
- On-Chip DACs for bias current and voltages
- Control circuit derived from HELIX128-3.1:
  - Consists of standard cells
  - Synthesized from Verilog description
- SEU robust (to be implemented in a later Version):
  - Triple redundant flip-flops
  - Register with ECC

Beetle1.1: Fixed Errors



Beetle1.1: Fixes & Improvements

- Working tristate buffers
  - Readable setup registers
- Biasing of Pipeline Readout Amplifier
- Fixed dummy transistors in transmission gates
- Missing ground connections added
- Analog delay circuit for I^2C Interface
  - Programming independent from 40MHz clock

Beetle1.2: Planned Features

- SEU robust control circuits
- faster frontend with lower noise etc.
- Mask register for test pulse
- Working readout daisy-chain
- "Orthogonalized" readout modes
  - Analog or binary operation
  - Multiplexing to 1,2 or 4 lines
  - optional "double data rate" operation with additional mux switch on (lines/2) ports
- Only one type of reset
- Error encoding in PCN
- JTAG boundary scan path
- Usefull "Error" signal

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Beetle: Chip History

Chip Name	Submission Date	Die Size [mm^2]	Description
BeetleFE10	May 1999	2×2	Frontend Testchip
BeetleBG10	May 1999	2×2	Bias Generator Testchip
Beetle10	April 2000	5.5×6.1	Complete Readout Chip
BeetleCO10	April 2000	2×2	Comparator Testchip
BeetlePA10	April 2000	2×2	Pipeline Amplifier Testchip
BeetleMA10	April 2000	2×2	MAPMT FE Testchip
Beetle11	March 2001	5.5×6.1	Complete Readout Chip
BeetleFE11	May 2001	2×2	Frontend Testchip
BeetleFE12	May 2001	2×2	Frontend Testchip
BeetleSR10	May 2001	2×2	SEU Robustnes Testchip
Beetle1.2	Q1/Q2 2002	5.5×6.1	Complete Readout Chip

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