0.1 Total Ionising Dose Irradiation Test

In total 5 boards were irradiated at the X-ray irradiation facility of CERN's microelectronic group.

For comparator studies (NIKHEF):

- 1 *Beetle1.4* up to 10 Mrad(SiO_2)
- 1 *Beetle1.5* up to 10 Mrad(SiO_2)

For DAC measurements, analogue performance test, noise studies (Heidelberg):

- 1 *Beetle1.3* up to 10 Mrad(SiO_2)
- 1 *Beetle1.5* up to 10 Mrad(SiO_2)
- 1 *Beetle1.5* up to 130 Mrad(SiO_2)

0.1.1

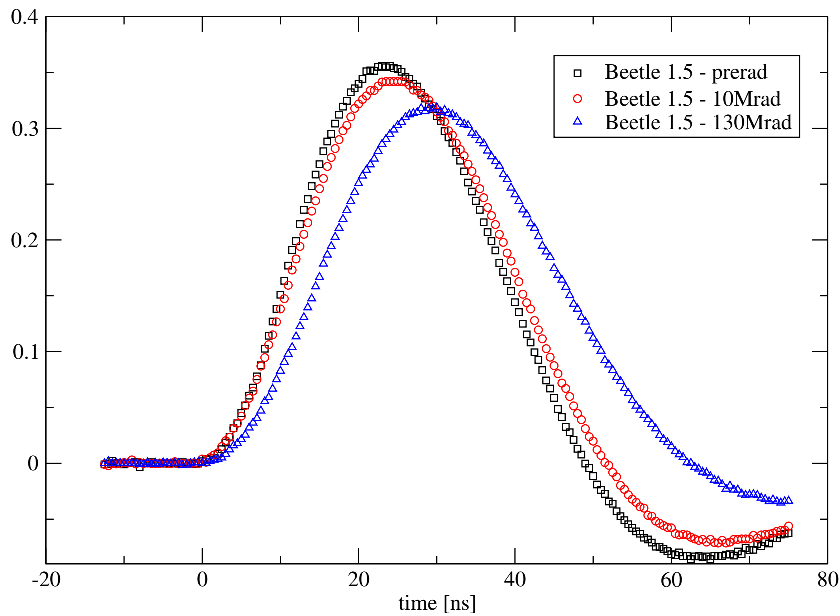

Figure 1: Pulse shape behaviour of a *Beetle1.5* under irradiation with X-ray for different total dose rates.

The peaking time of the prerad chip is around 22 ns. and increase up to 24 ns for the 10 Mrad irradiated chip. For the 130 Mrad *Beetle* the peaking time is around 30 ns and there is a clear degradation in gain, remainder after 25 ns and undershoot visible.

0.1.2 Pulse shape and annealing

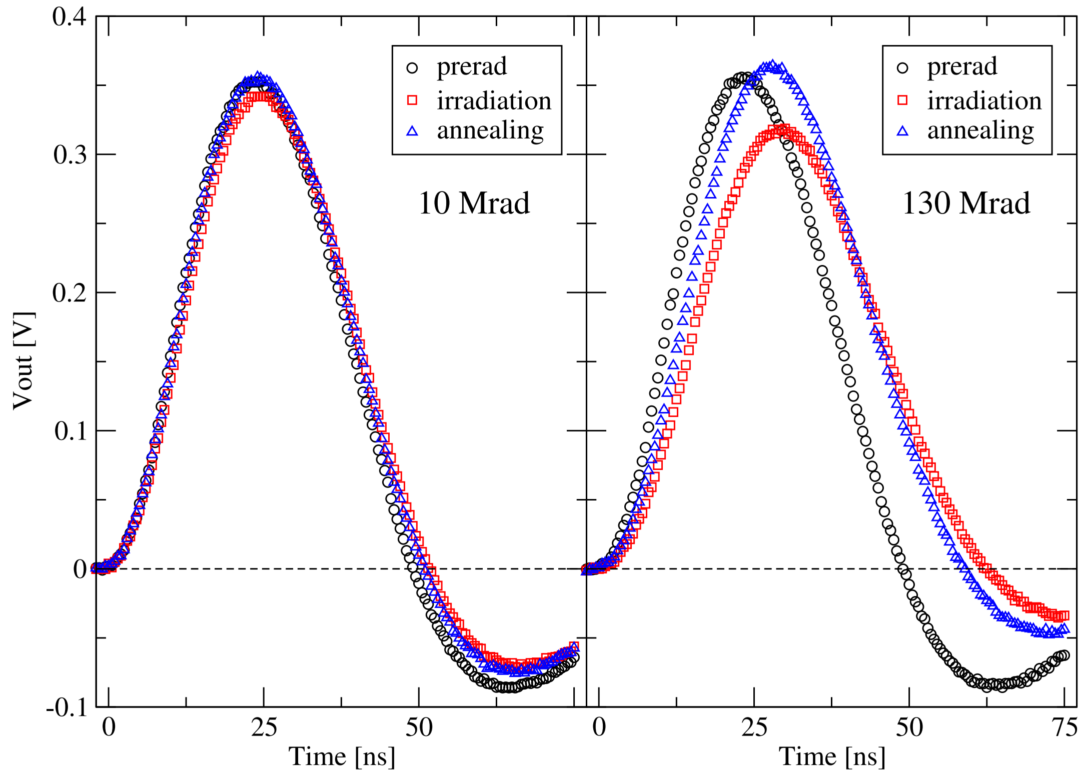

Figure 2: Pulse shape variation of two *Beetle1.5* chips before and after irradiation as well as after annealing at 100℃. In the left diagram the chip was irradiated up to a total dose of 10 Mrad(SiO_2) and up to 130 Mrad in the right plot.

0.1.3 Readout baseline

The readout for all measurements were done in the 4 port readout mode (LHCb mode) and added together to one baseline plot.

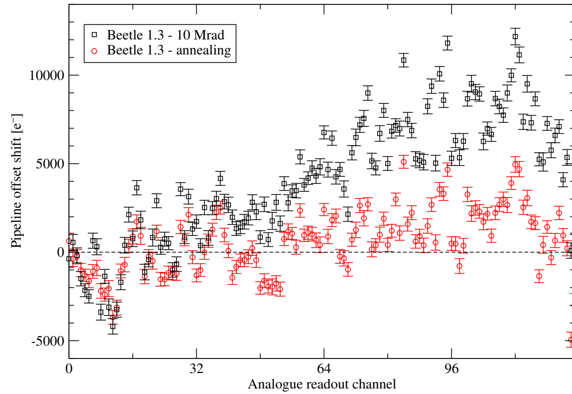

Figure 3: Pipeline offset shift of *Beetle1.3* after irradiation (10 Mrad) and after annealing.

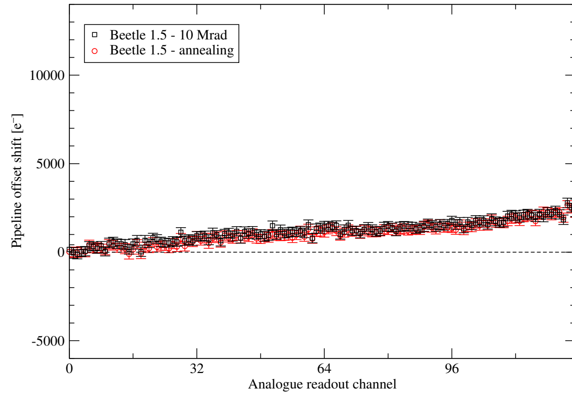

Figure 4: Pipeline offset shift of *Beetle1.5* after irradiation (10 Mrad) and after annealing.

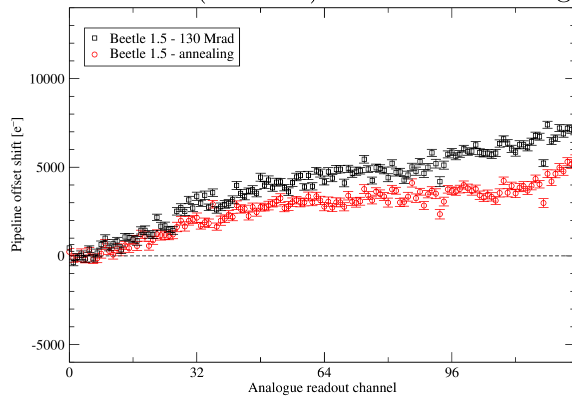

Figure 5: Pipeline offset shift of *Beetle1.5* after irradiation (130 Mrad) and after annealing.

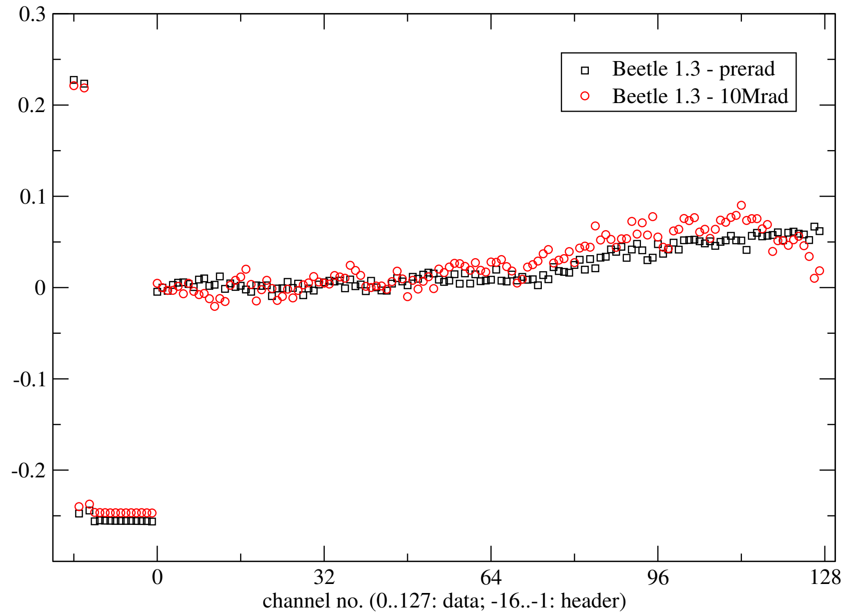

Figure 6: Readout baseline of a *Beetle1.3* before and after irradiation with X-rays.

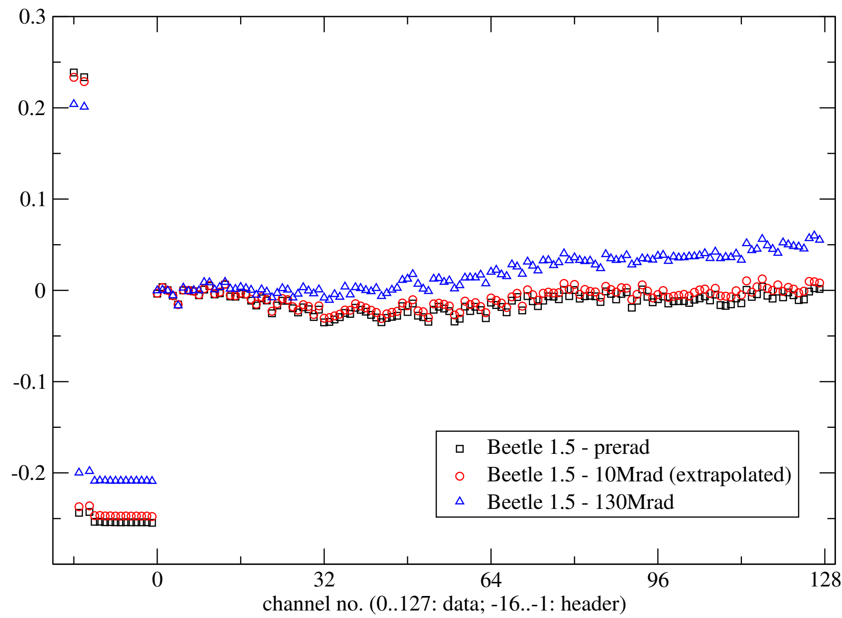

Figure 7: Readout baseline of a *Beetle1.5* before and after irradiation with X-rays.

Possible explanation: The major differences between *Beetle1.3* and *Beetle1.5* is the new pipeline structure. For *Beetle1.5* there is a n-well under nmos gate-capacitor of the pipeline. The front-end can be excluded as the source of the difference; the pulse shape analysis of both irradiated chips (1.3 and 1.5) are identical.

0.1.4 Equivalent Noise Charge (ENC)

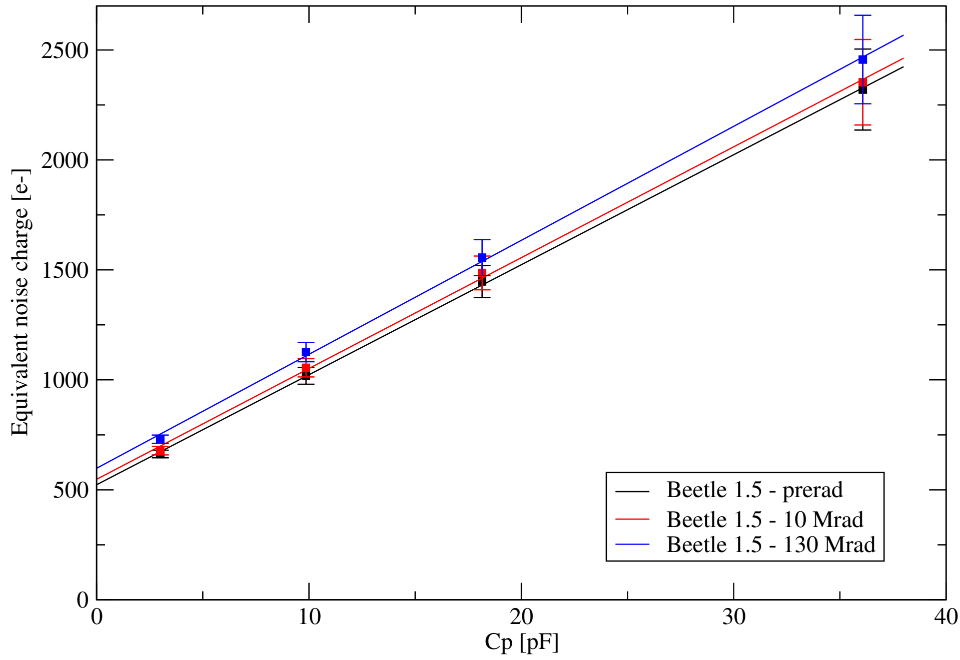

Figure 8: Equivalent noise charge as function of the load capacitance and dose.

Integral dose	Equivalent noise charge
0 Mrad (prerad)	$\mathrm{ENC} = 523.20\,\mathrm{e}^- + 49.99\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
10 Mrad	$\mathrm{ENC} = 547.60\,\mathrm{e}^- + 50.40\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
130 Mrad	$\mathrm{ENC} = 597.81\,\mathrm{e}^- + 51.83\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$

Table 1: Measured equivalent noise charge of *Beetle1.5* for different dose levels.

0.1.5 ProbeIDAC

`ProbeIDAC` is a current mirrored test port of the register `Ibuf`. This pad is only available on a *Beetle1.3* ar *tle1.3* and after 1(

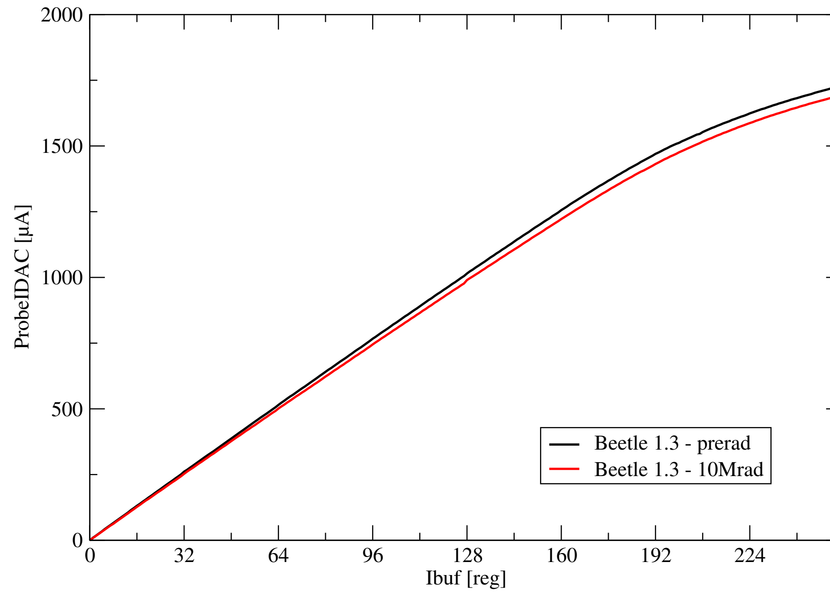

Figure 9: Behaviour of the test node `ProbeIDAC` of a *Beetle1.3* before and after X-ray irradiation.

Possible reasons for this effect:

- degradation of the common current source of the *Beetle*
- degradation of the current DAC

The current degradation after 10 Mrad is around 2.4% of the prerad current measurement.

0.2 Process Parameter Test(PPT)

Description (Gate Length)	Description (Speed)	Exposure	L_{poly} delta (nm)	L_{poly} delta (sigma)	Corner
Very Short	Very Fast	85% of Nominal	−30 nm	$\sim -3.0\,\sigma$	+3.0
Short	Fast	92% of Nominal	−15 nm	$\sim -1.5\,\sigma$	+1.5
Nominal	Nominal	100% of Nominal	Nominal	Nominal	0
Long	Slow	115% of Nominal	+15 nm	$\sim +1.5\,\sigma$	−1.5
Very Long	Very Slow	125% of Nominal	+30 nm	$\sim +3.0\,\sigma$	−3.0

Table 2: Explanation of process parameters variations. L_{poly} is the same as L_{eff} (effective length). Short L_{eff} translates into 'fast process', whilst long L_{eff} in 'slow process'. The L_{eff} variation is indicated as percent of exposure (85 to 125%), and the correspondence between exposure and 'fast' or 'slow' process is shown. Column 'Corner' indicates the comparable settings for simulations.

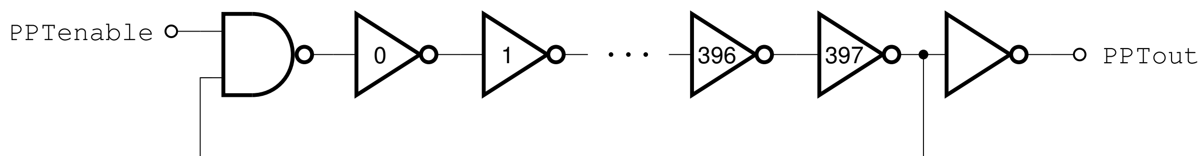

Figure 10: Schematic of the *Beetle1.5* Process Parameter Test.

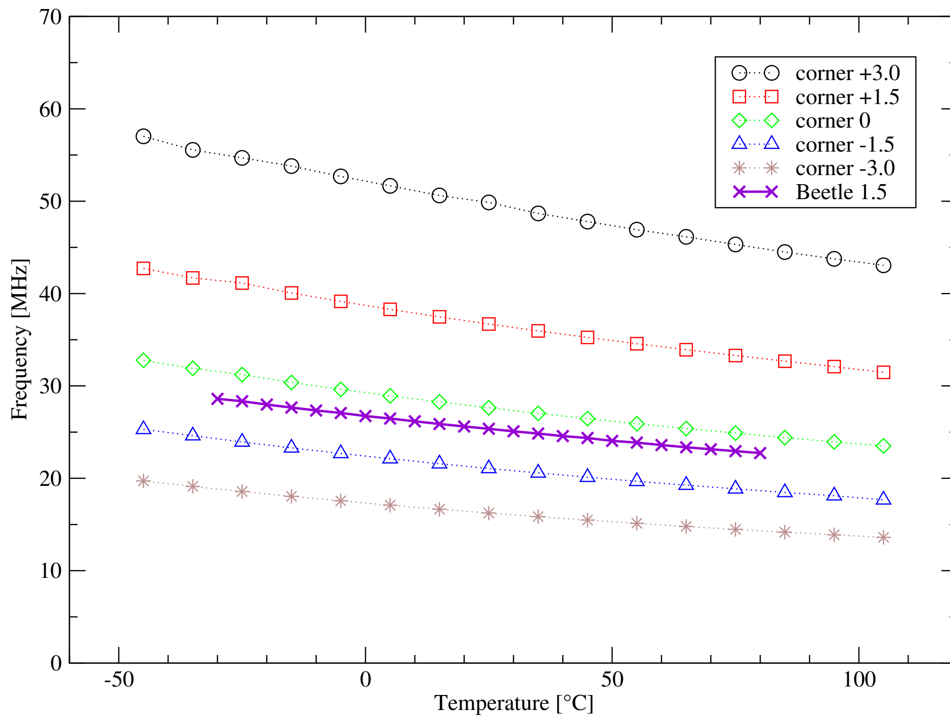

Figure 11: Simulation and test results of the *Beetle1.5* Process Parameter Test. The dashed lines are simulation results for different corner parameters (-3 to $+3$) while the solid line is from a measurement of a *Beetle1.5* chip diced from wafer KSMNKAT.

0.2.1 Test Channel

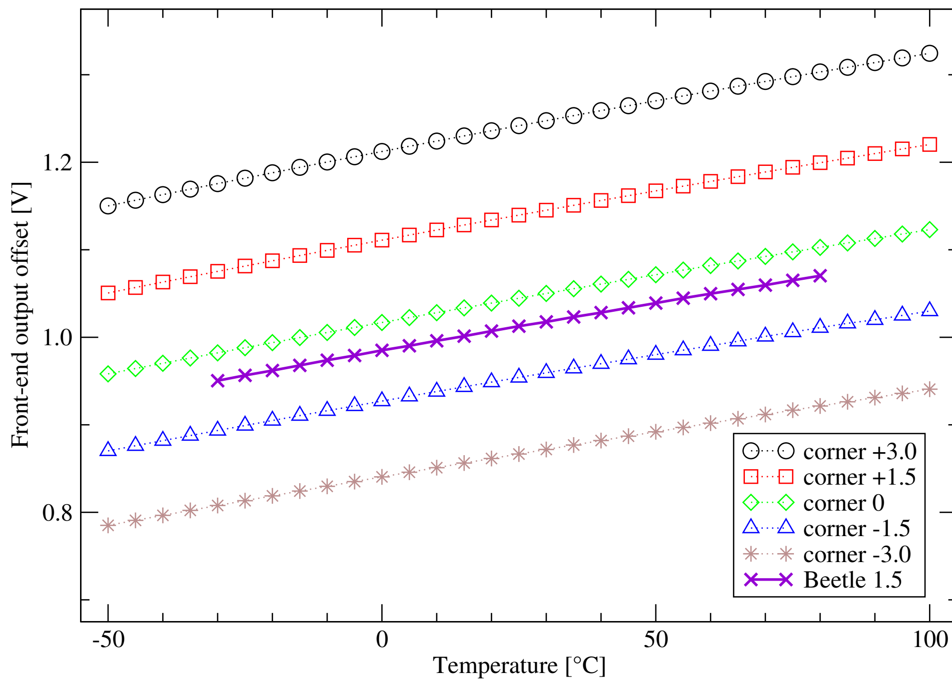

Figure 12: Simulation and test results of the front-end output offset. The dashed lines are simulation results for different corner parameters (from -3 to $+3$) and temperatures (from -50℃ to $+100$℃) while the solid line is from a measurement of a *Beetle1.5* chip diced from wafer KSMNKAT.

0.3 'Manually operated' Mass Production Tests

0.3.1 Set-up

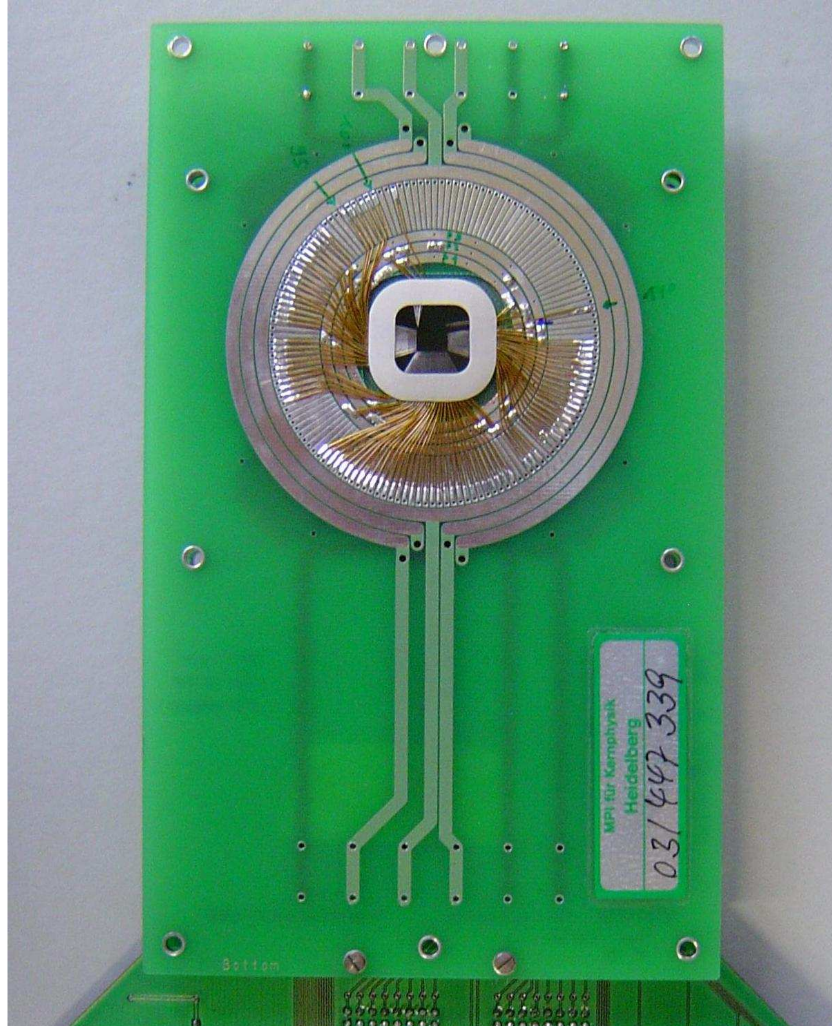

Figure 13: Sub-side view of the *Beetle* probe card. The 129 needles can be recognized in the middle of the white ring.

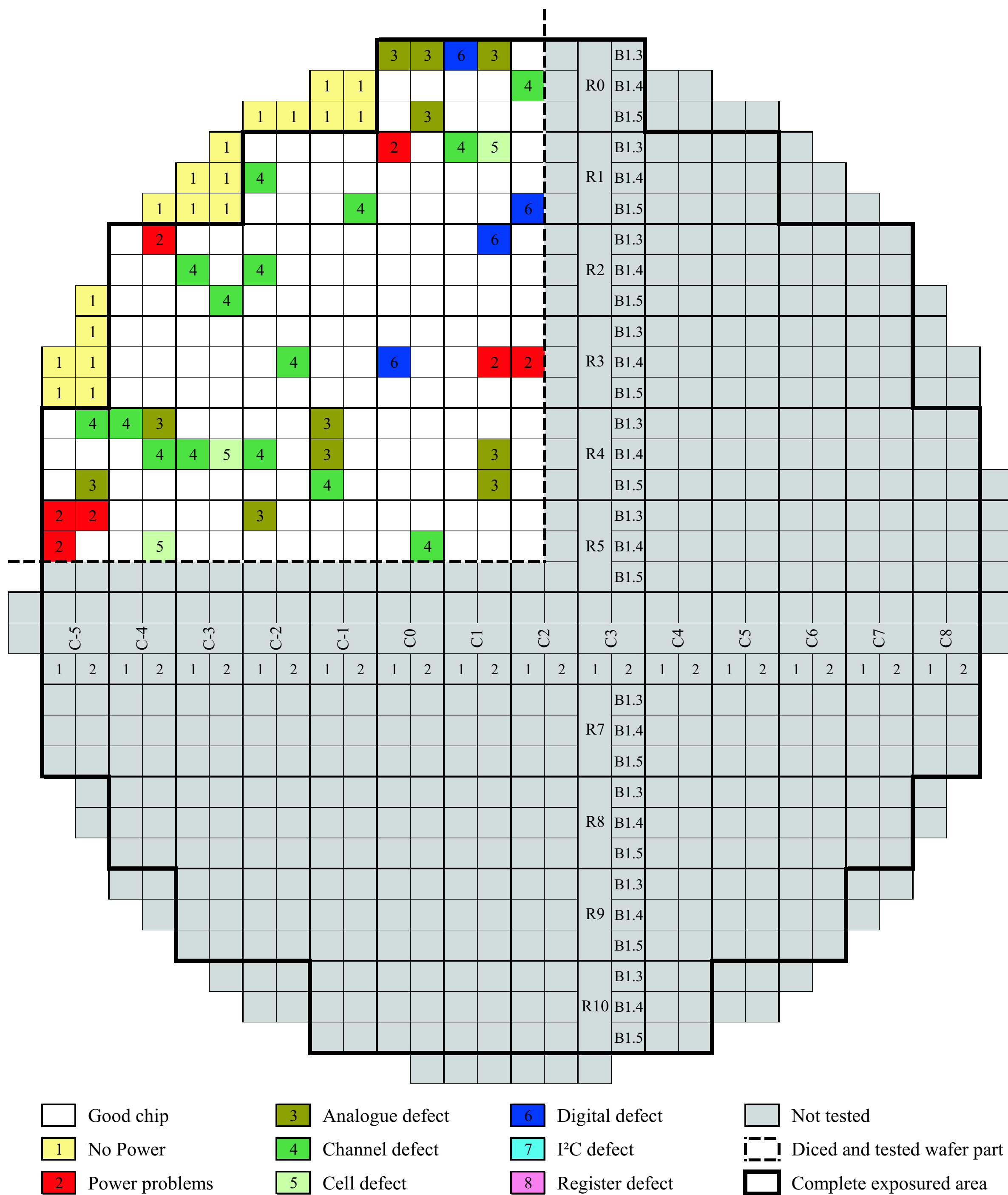

Figure 14: Wafer map of a *Beetle* Engineering Run wafer. Shown is the whole wafer with 790 dies. Different chip versions are ordered in rows. Framed chips in groups of up to six chips are from the same reticle and so exposed during wafer production simultaneously. The upper left quarter represents the tested area of wafer KSMNKAT. Defects are marked with different colours. Obviously chips with no power consumption (inked yellow) are from the same exposure step, because the defects are restricted only to this area. One expects the same problems with these chips on different wafers from the same fabrication run.

0.3.2 Yield

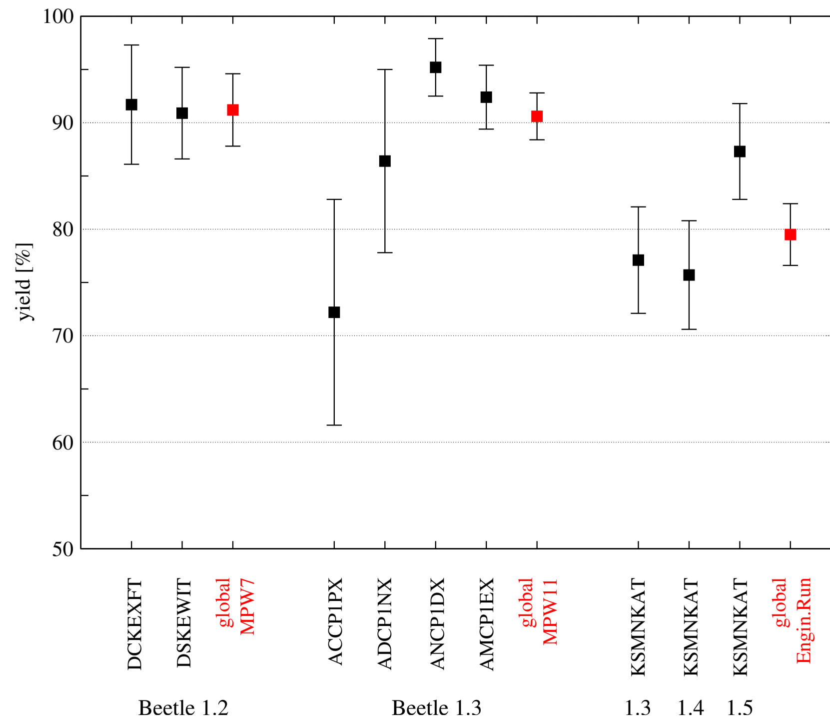

Figure 15: Summary of all mass production test results. For comparison reasons two results from a former chip test are included (*Beetle1.2* chips from MPW 7). A global value is added to the diagram for each different production lot (red dots).

0.3.3 Process Variation

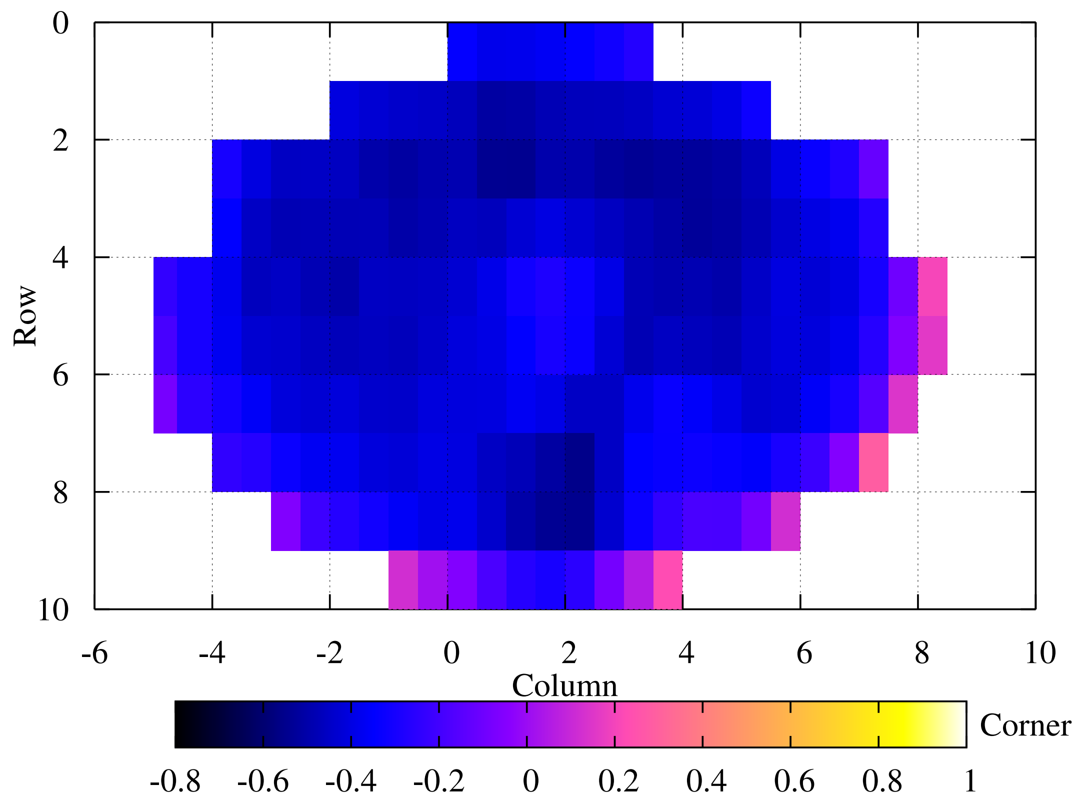

Figure 16: Distribution of measured *Corner* parameters over wafer K2MNG2T.

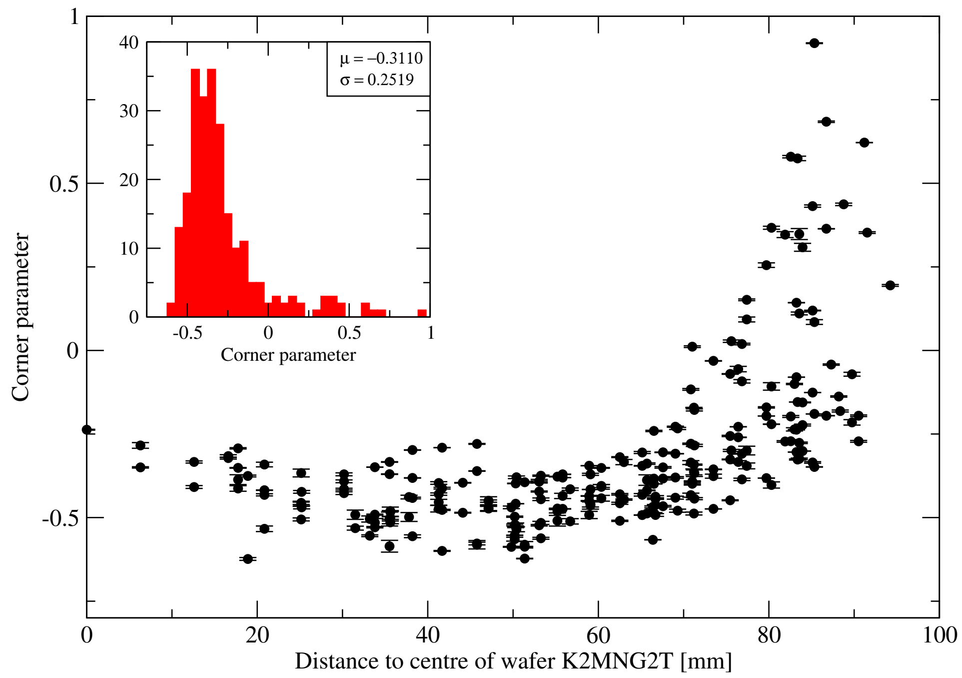

Figure 17: *Corner* parameter distribution as a function of the distance to the centre of wafer K2MNG2T. The histogram of the *Corner* distribution is also shown in the diagram.

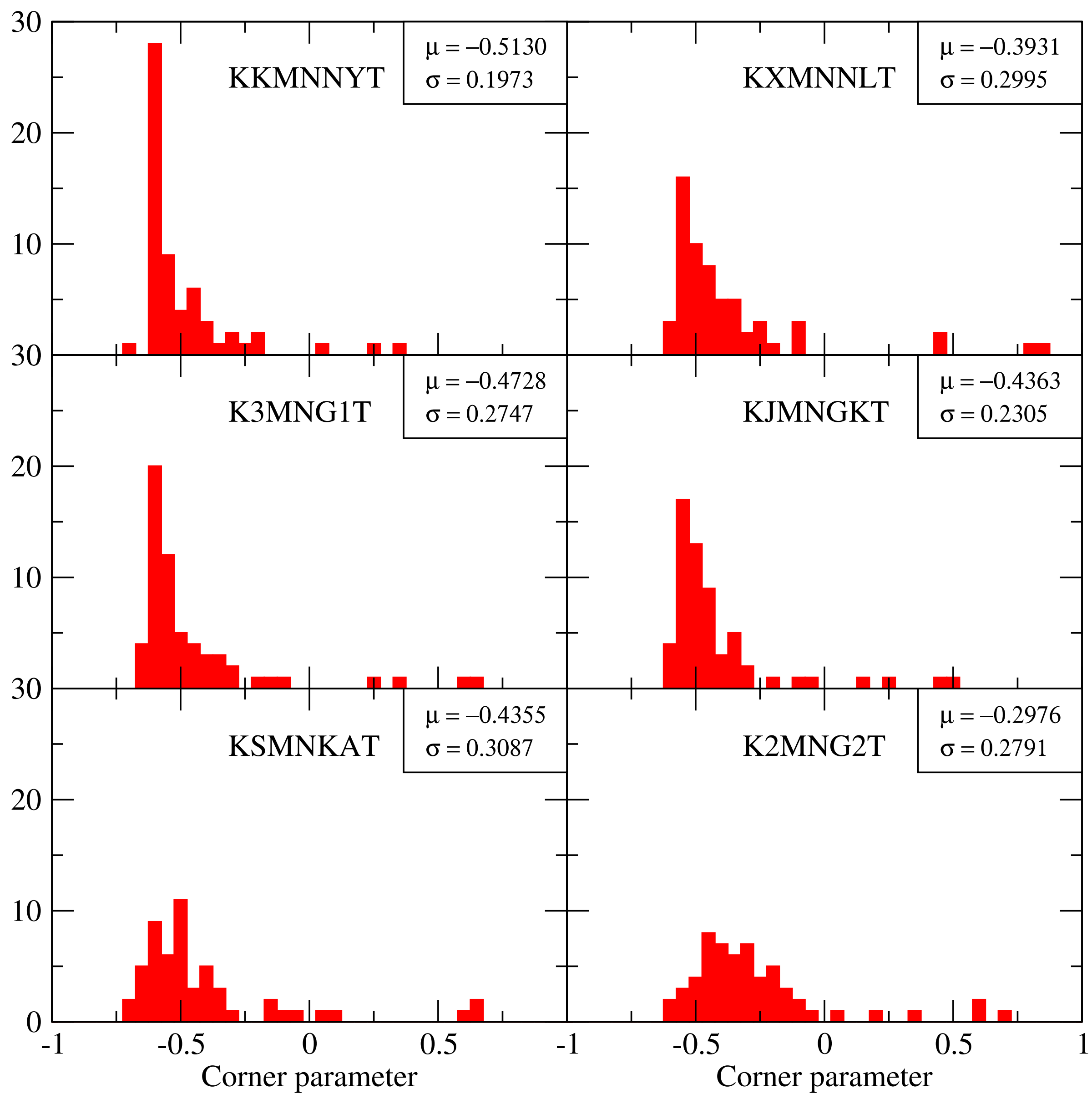

Figure 18: Histogram of the *Corner* variation for all wafers of the Engineering Run. The mean value and the standard deviation of the process parameters for each wafer number is quoted in the diagram.

Sven Loechner, June 3, 2005