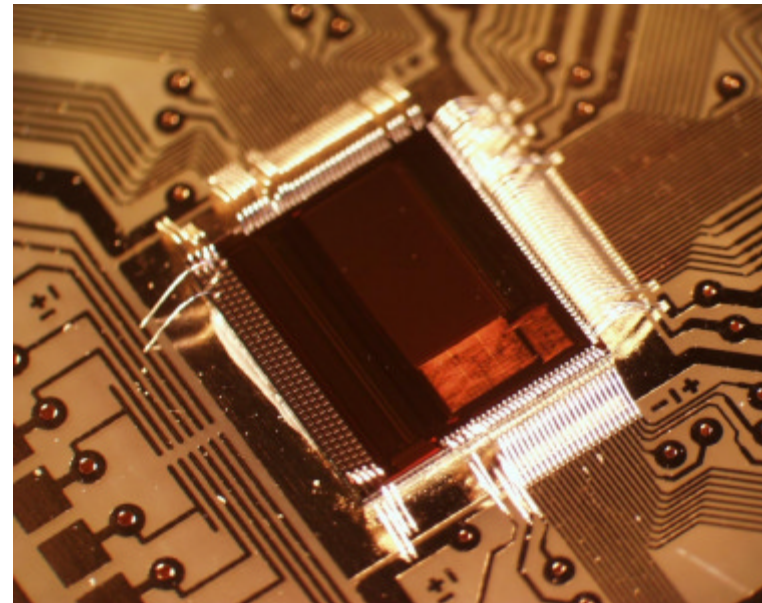




# SEU beam test FIB patch

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Beetle 1.3 on a test PCB





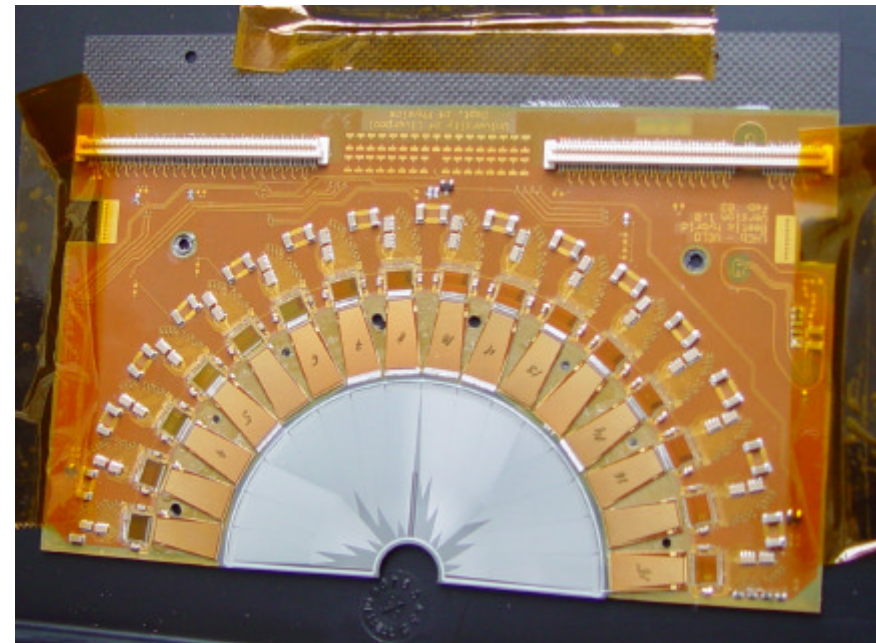
# Outline

- **SEU beam test**

- setup
- results

- **FIB patch**

- problem
- patch solution
- FIB
- lab-tests



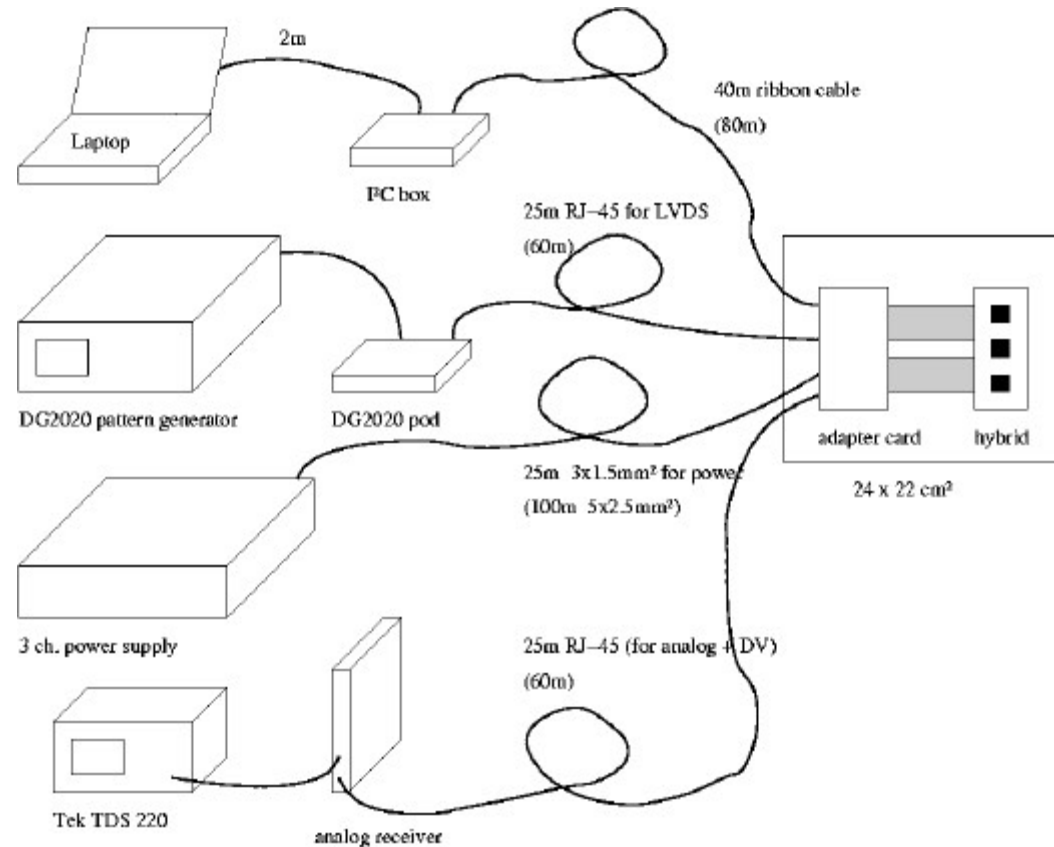
16 Beetle 1.3 on a VELO hybrid attached to Si-sensor





# SEU beam test (1)

- SEU beam test at **Proton Irradiation Facility (PIF)** Paul-Scherrer Institute, CH
- Irradiation of 3 Beetle chips:
  - 65 MeV protons
- Check for bit-flips in Beetle registers
  - SEU cross section for a std. flip-flop



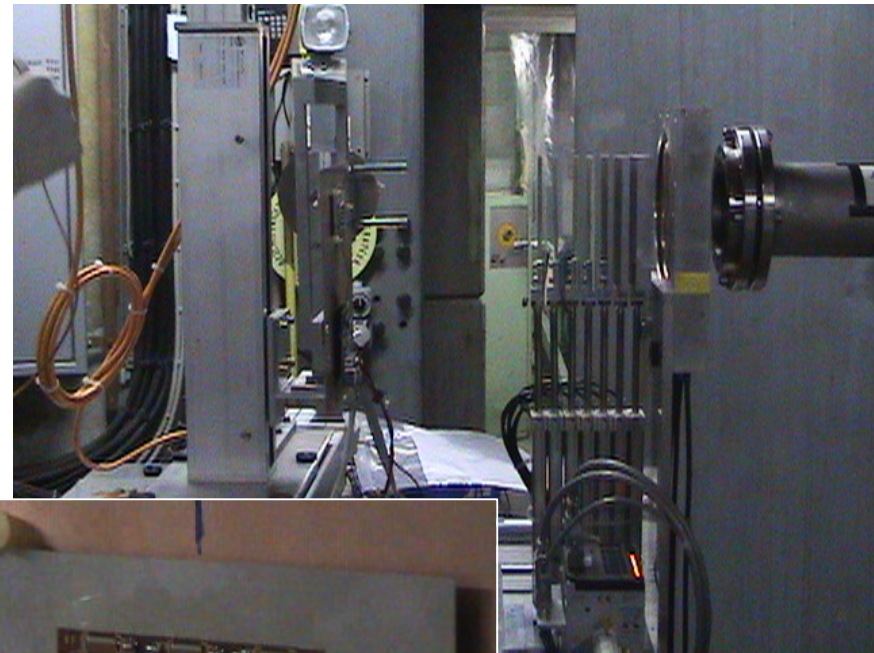




# SEU beam test (2)



setup on top of the irradiation facility





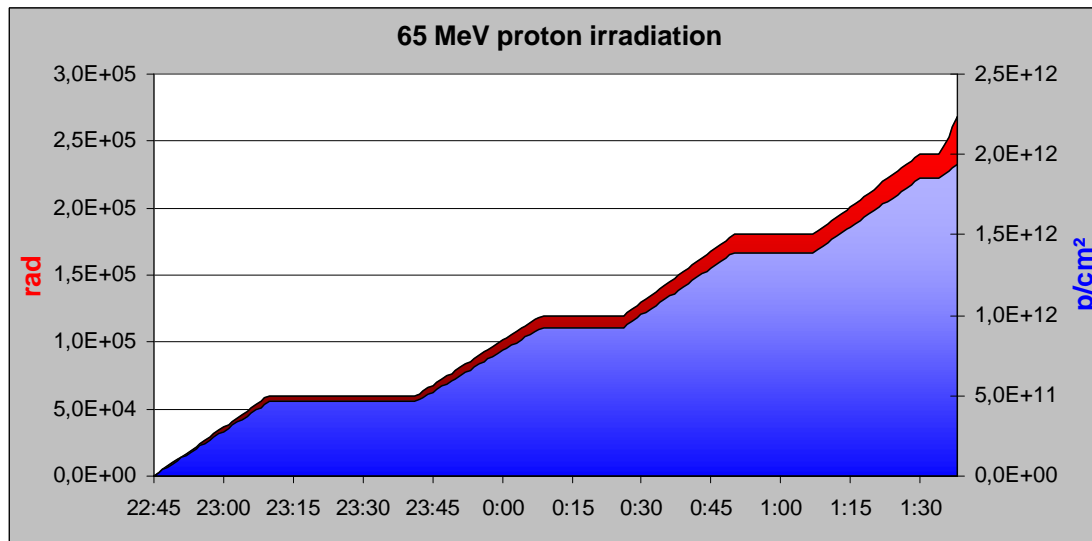
# SEU beam test (3)

## • First irradiation (Tu. - Wed.):

- 65 MeV protons
- mean flux:  $3.13 \times 10^8$  p/cm<sup>2</sup>/s
- fluence:  $1.95 \times 10^{12}$  p/cm<sup>2</sup>
- accumulated dose: 273 krad

## • estimated cross section per FF: $10^{-13}$ to $10^{-15}$ cm<sup>2</sup>

- 1 SEU every 300 s ( $10^8$  p/cm<sup>2</sup>/s)
- +/- 1 magnitude



**but no SEU bit flips found**



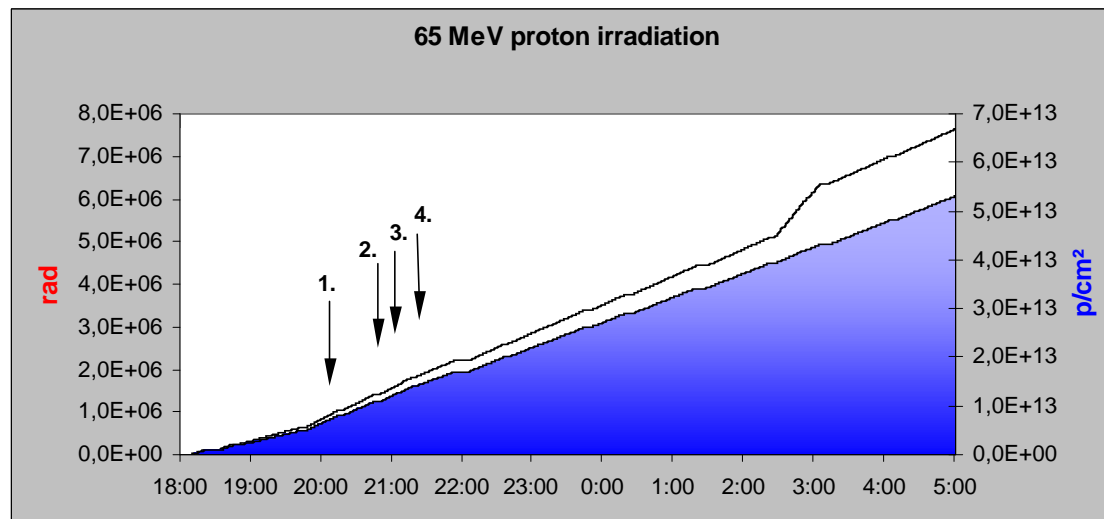


# SEU beam test (4)

## ● Second irradiation (Th. - Fr.):

- 65 MeV protons
- mean flux:  $1.56 \times 10^9$  p/cm<sup>2</sup>/s
- fluence:  $5.31 \times 10^{13}$  p/cm<sup>2</sup>
- accumulated dose: 7.66 Mrad

- 4 SEU flips found
- time distribution not yet understood



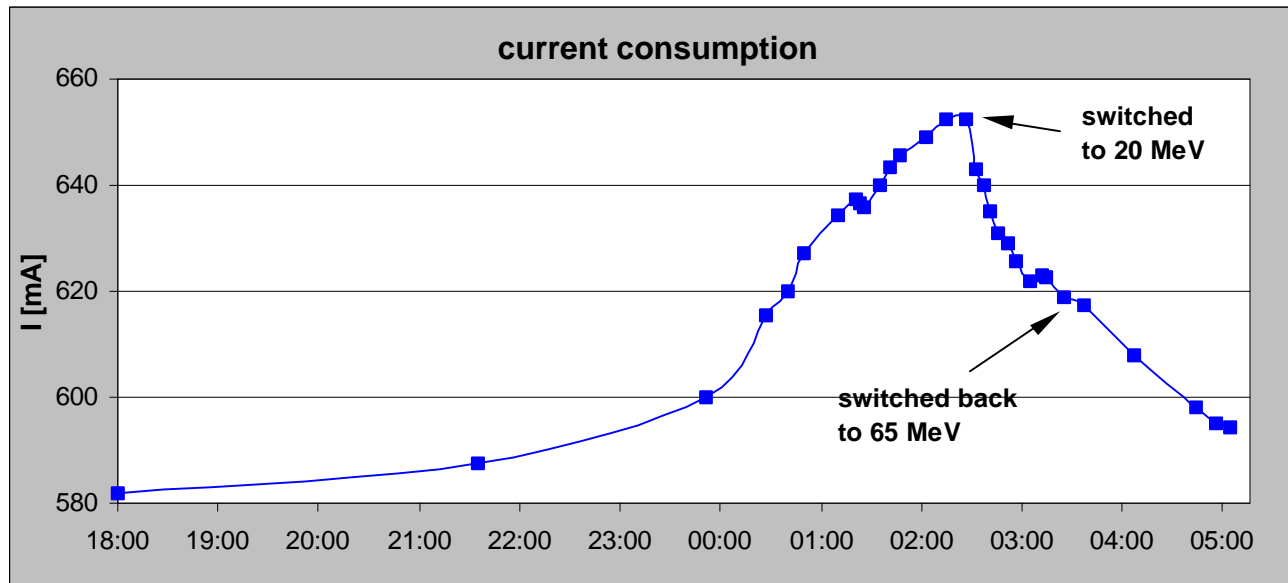
- Pulse shape scan:
  - no variation of pulse before / after irradiation





# SEU beam test (5)

## Current consumption of all 3 Beetle chips



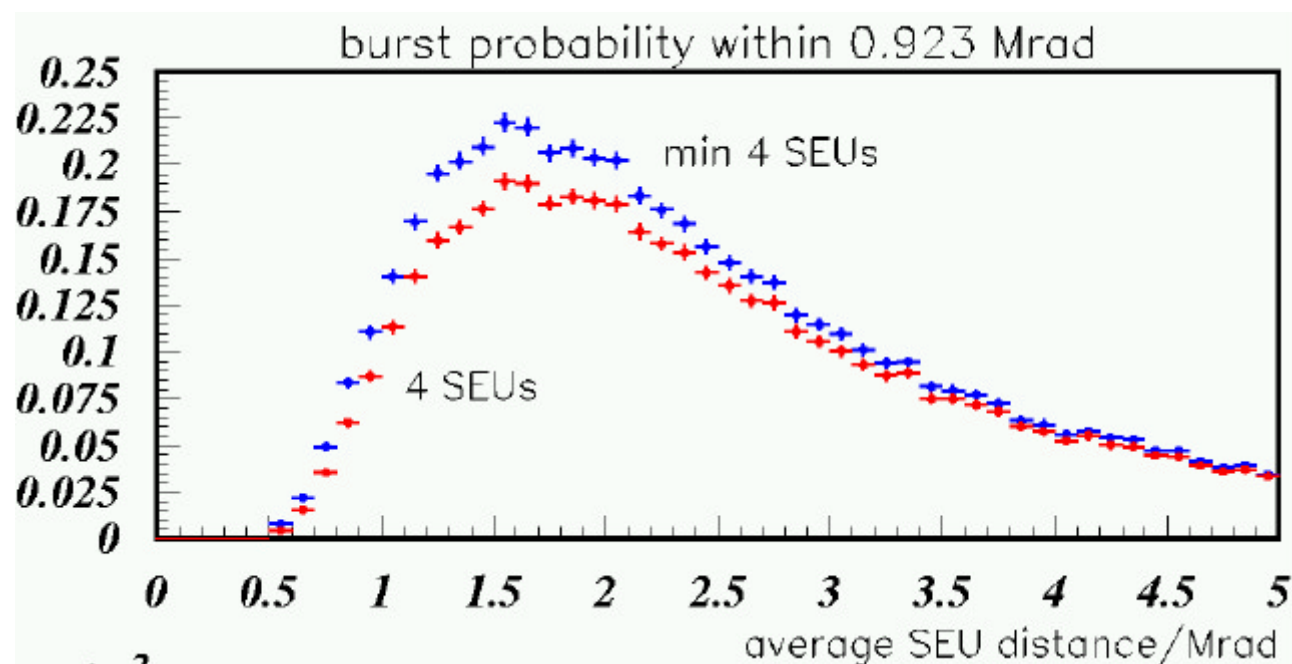
behaviour not yet understood





# SEU beam test (6)

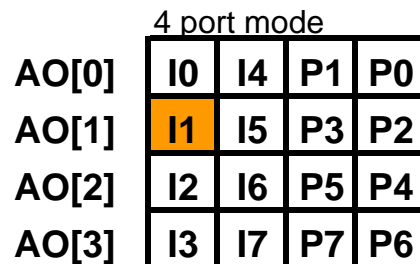
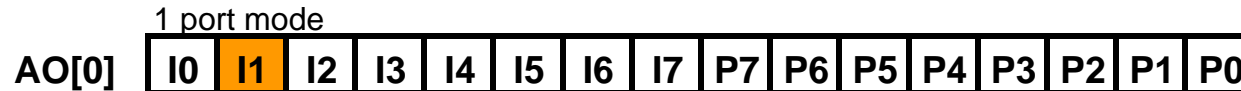
- probability of a burst of 4 SEUs (or more) in a window of 0.923 Mrad:
  - 4 SEU: 0,2 % probability... (unlikely...)







# Readout header: parity bit



- I0 leading bit (always 0)
- I1 parity of PCN (even)
- I2 Active EDC
- I3 parity of reg. CompChTh
- I4 parity of reg. CompMask
- I5 parity of reg. TpSelect
- I6 SEU counter <1>
- I7 SEU counter <0>

- Parity bit (I1) is wrong encoded in 4 port mode and Rclk divider = 0 (LHCb mode)

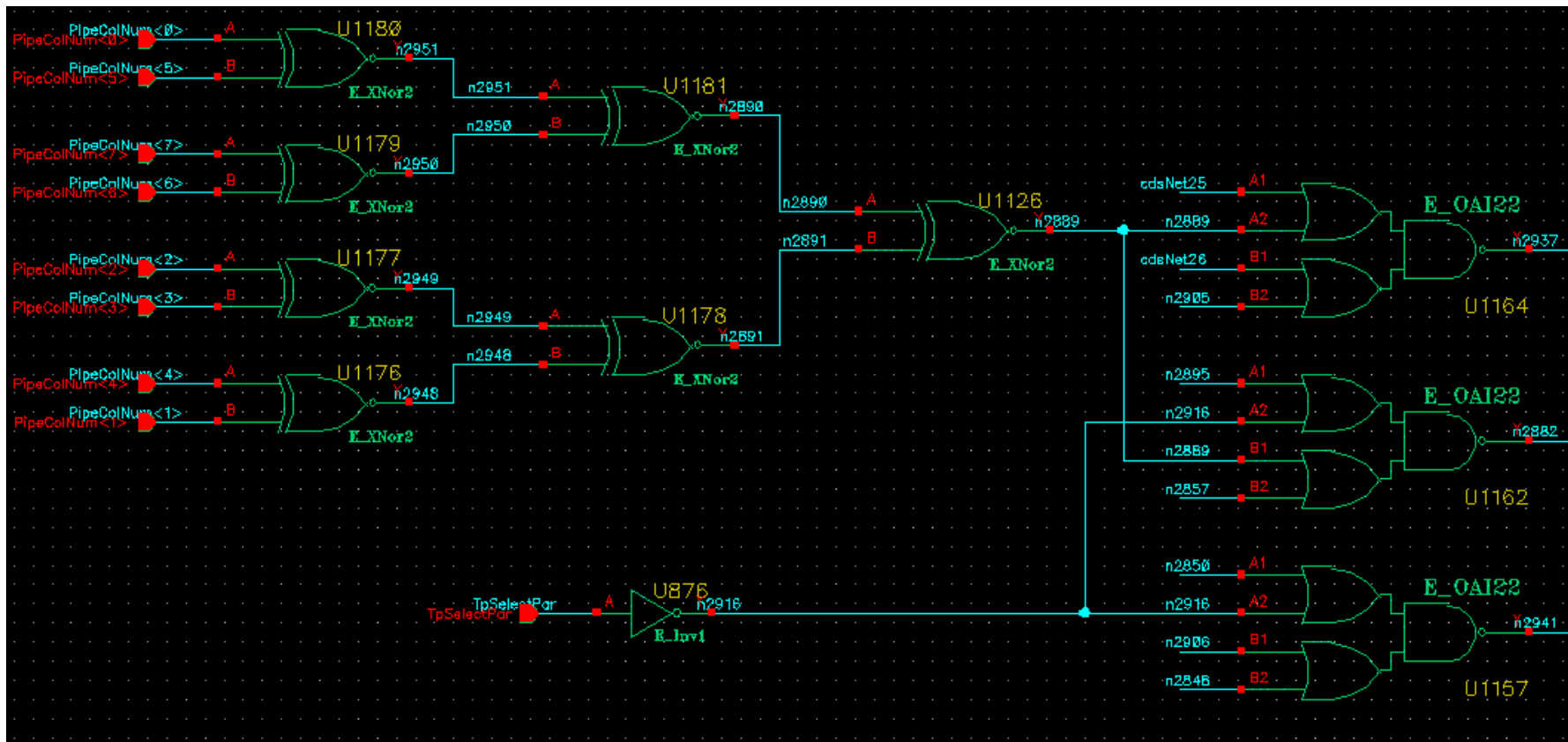
all other modes or Rclk divider settings  
→ Parity bit is OK

- problem is understood in verilog
  - not so easy to fix
  - simple workaround: swap position I1 with I5  
could be tested on a 1.3 with a FIB patch





# Parity bit - workaround (1)

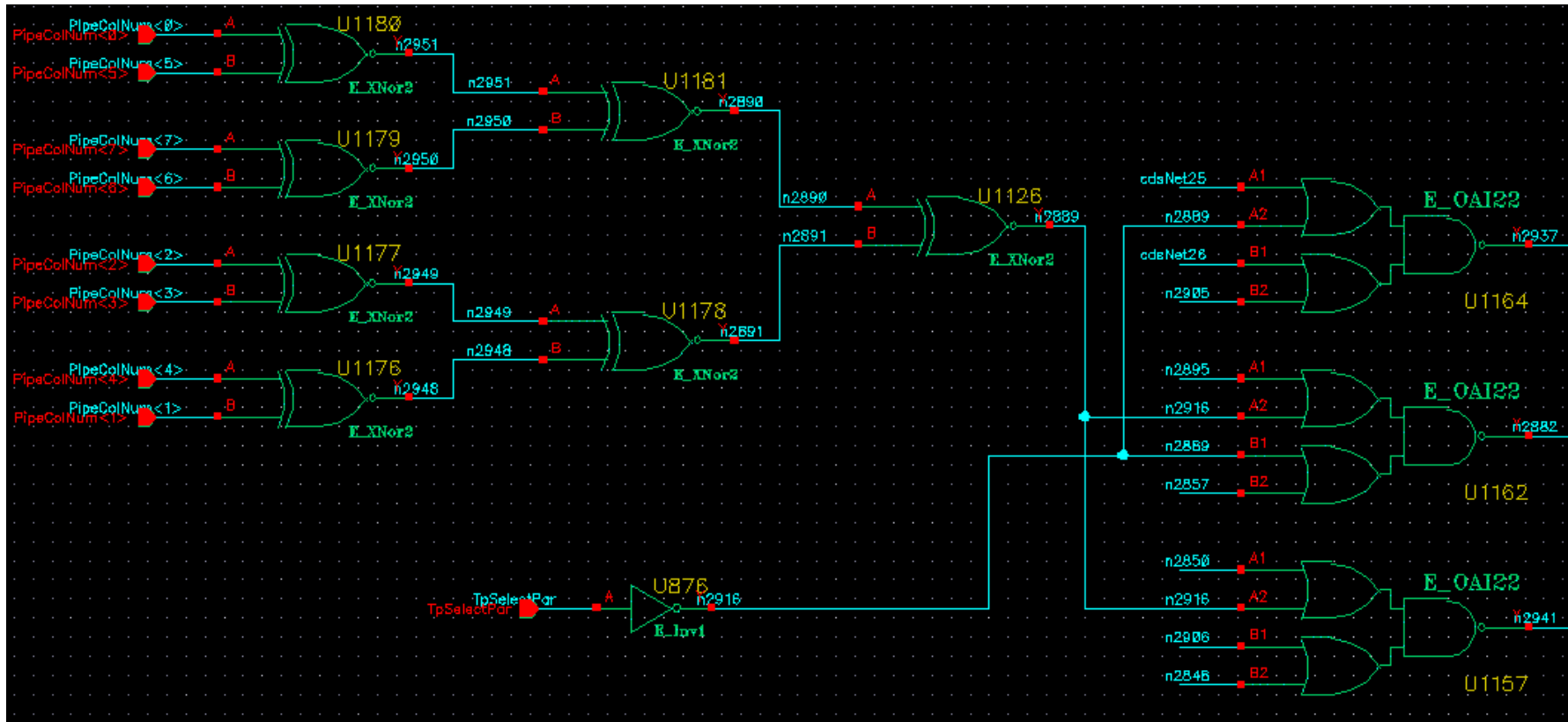


schematic of parity-bit generation (part of MuxScheduler)





# Parity bit - workaround (2)



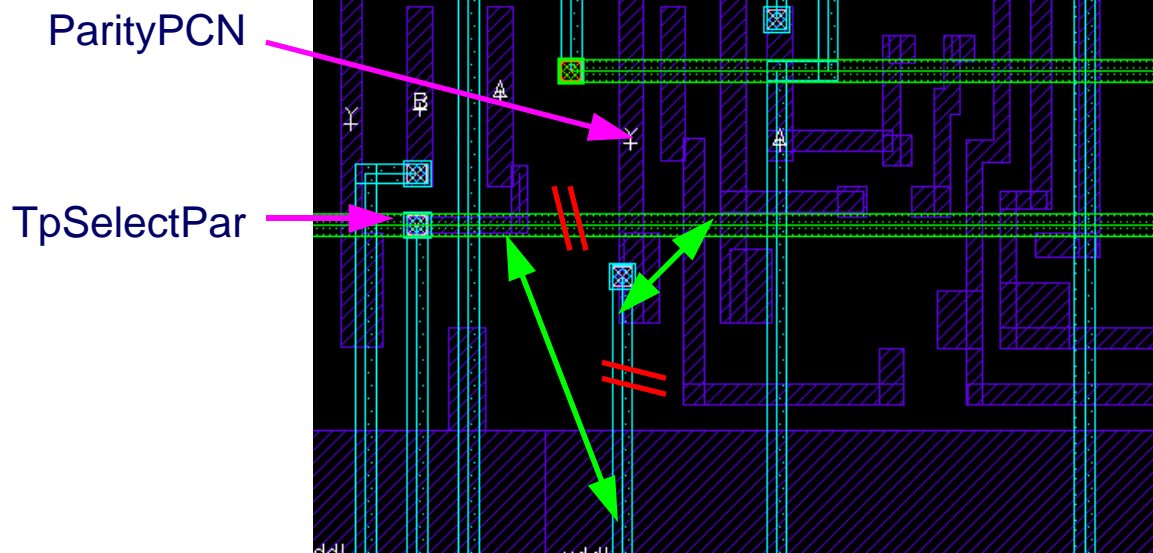
new schematic of parity-bit patch





# Parity bit - workaround (3)

- **Layout modification in FastControl of Beetle (could be done by a FIB)**
  - 2 cuts
  - 2 connections

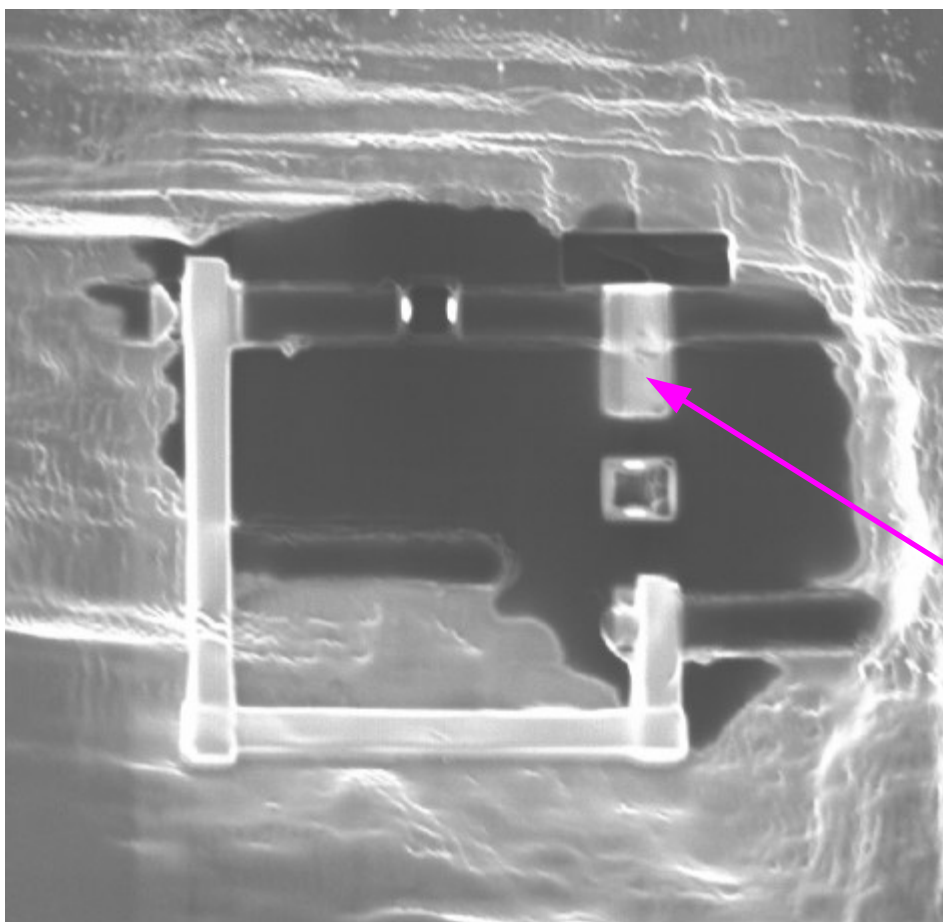


Output device of ParityPCN generation - E\_XNor2 (U1126)





# FIB patch (1)



- Swap header bit I1 with I5
- done with a FIB patch (FEICO Munich)

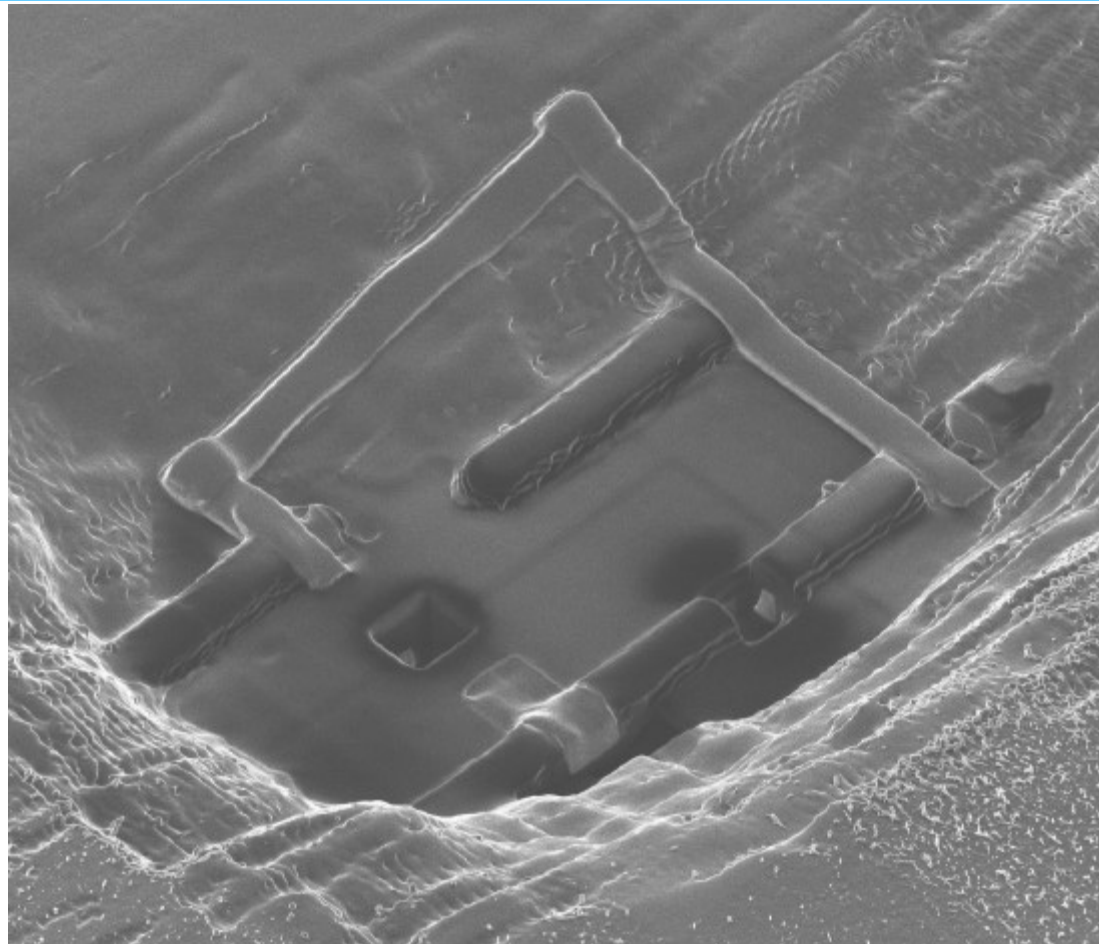
Output device of ParityPCN generation - E\_XNor2 (U1126)





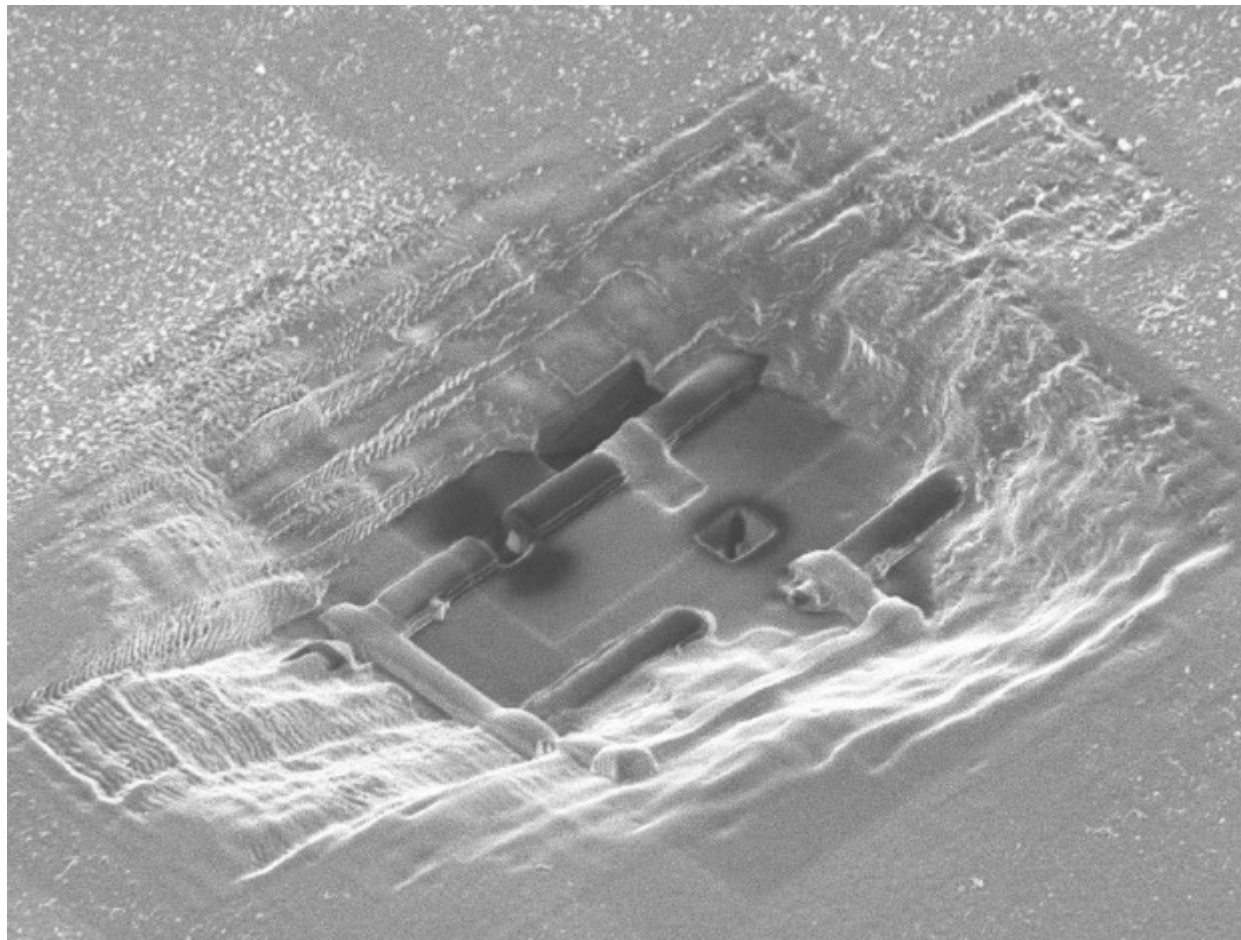


# FIB patch (2)





# FIB patch (3)





## FIB: results:

- **one patched Beetle 1.3 chip tested:**
  - $1 \times 10^6$  readouts in 1 port mode (Testmode)
  - $3 \times 10^6$  readouts in 1 port mode (LHCb mode)
  - non-consecutive / consecutive readouts
  - different Rclk divider settings
- **→ Parity bit is now right encoded**
  
- **asynchron trigger:**
  - $3 \times 10^6$  readouts
- **→ no hiccup of FastControl**

