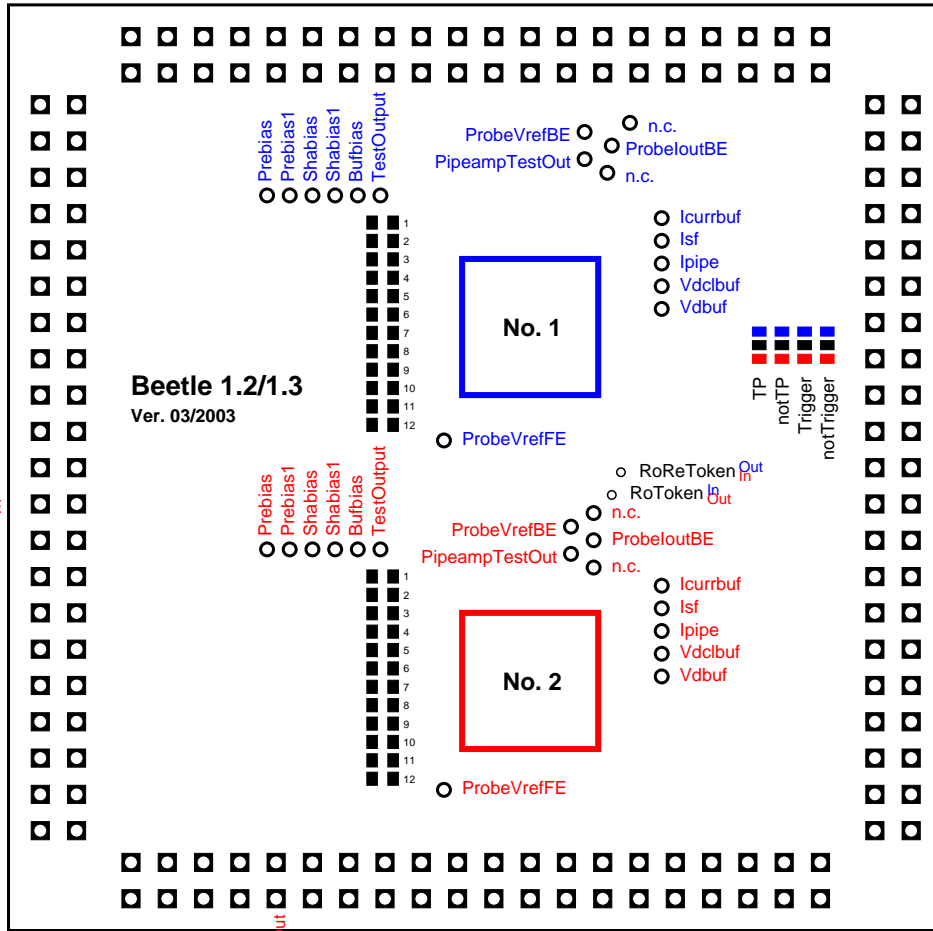


AI<1> AI<2>  
 AI<3> AI<4>  
 AI<5> AI<6>  
 AI<7> AI<8>  
 AI<9> AI<10>  
 AI<11> AI<12>  
 vdda notCompClk  
 CompClk CO<8>  
 notCO<8> CO<9>  
 notCO<9> CO<10>  
 notCO<10> CO<11>  
 notCO<11> ProbeloutBE  
 vdda gnd  
 vdda AI<1>  
 AI<2> AI<3>  
 AI<4> AI<5>  
 AI<6> AI<7>  
 AI<8> AI<9>  
 AI<10> AI<11>  
 AI<12> vdda  
 notCompClk CompClk



notCO<8> CO<8>  
 notCO<9> CO<9>  
 notCO<10> CO<10>  
 notCO<11> CO<11>  
 RoTokenIn RoReTokenOut  
 notCO<15> FifoFull  
 notCO<14> CO<15>  
 notCO<13> CO<14>  
 notCO<12> CO<13>  
 gndcomp CO<12>  
 EnableEDC vddcomp  
 gnd gnd  
 WriteMon TrigMon  
 Trigger notTrigger  
 Clock notClock  
 TP notTP  
 Reset notReset  
 DV notDV  
 gnd gnd  
 SDA SCL

vdda vdda  
 notCO<0> CO<0>  
 notCO<1> CO<1>  
 notCO<2> CO<2>  
 notCO<3> CO<3>  
 notCO<4> CO<4>  
 notCO<5> CO<5>  
 notCO<6> CO<6>  
 notCO<7> CO<7>  
 gnd gnd  
 RoReTokenIn RoTokenOut  
 vddcomp gndcomp  
 vddd vdda  
 I2CAAddr<0> gndd  
 I2CAAddr<2> I2CAAddr<1>  
 I2CAAddr<4> I2CAAddr<3>  
 I2CAAddr<6> I2CAAddr<5>  
 notAO<0> AO<0>  
 notAO<1> AO<1>  
 AO<3> notAO<3>

AO<2> notAO<2>  
 notDV DV  
 notTP TP  
 notTrigger Trigger  
 TrigMon WriteMon  
 vddcomp EnableEDC  
 CO<12> gndcomp  
 CO<13> notCO<12>  
 CO<14> notCO<13>  
 CO<15> notCO<14>  
 FifoFull notCO<15>  
 vddcomp gndcomp  
 vddd vdda  
 I2CAAddr<0> gndd  
 I2CAAddr<2> I2CAAddr<1>  
 I2CAAddr<4> I2CAAddr<3>  
 I2CAAddr<6> I2CAAddr<5>  
 notAO<0> AO<0>  
 notAO<1> AO<1>  
 AO<3> notAO<3>  
 AO<2> notAO<2>