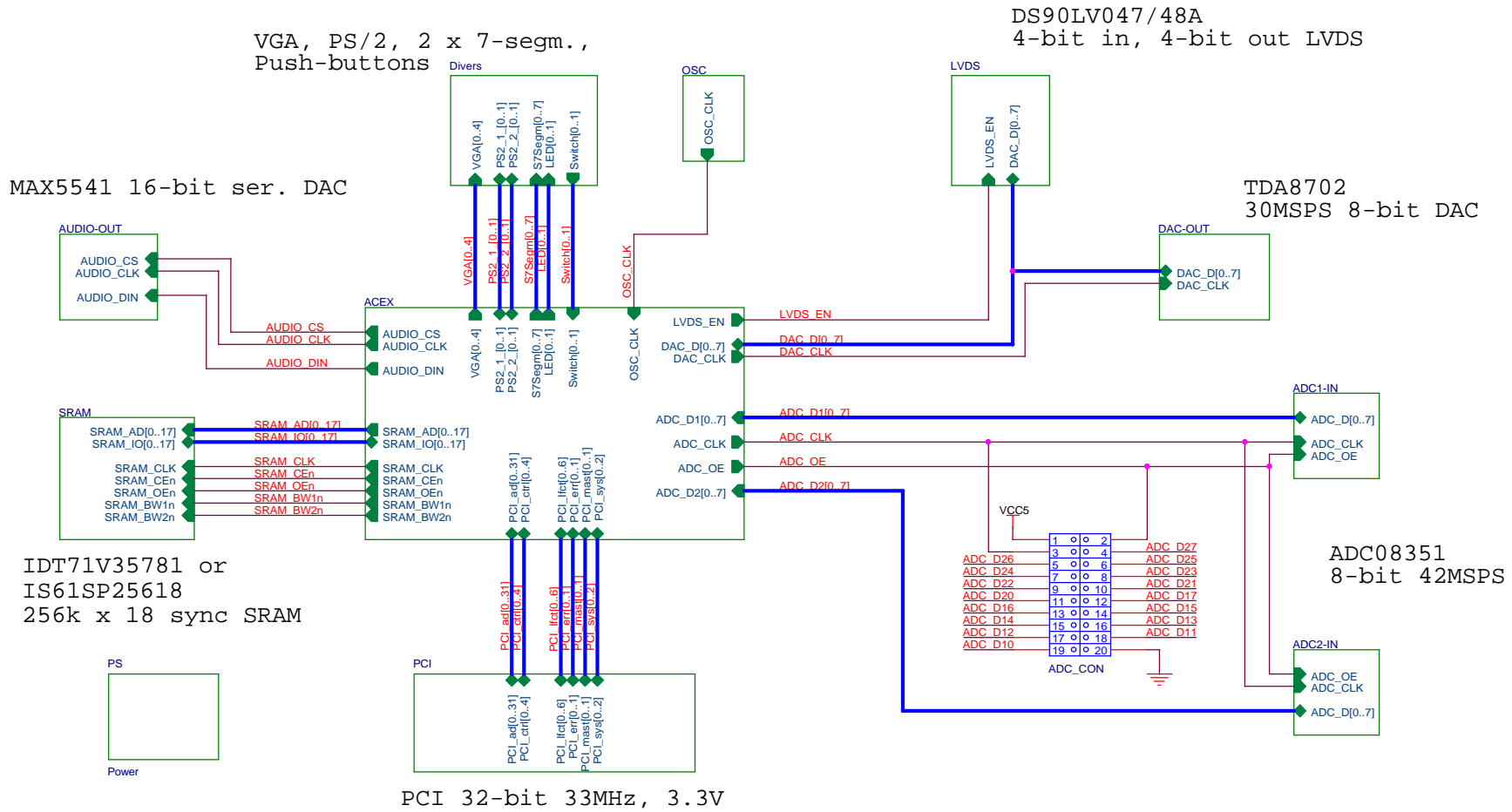
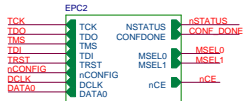


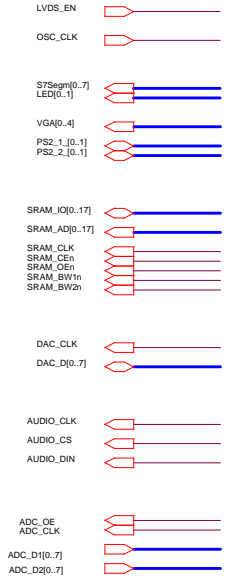
ACEX-KIP Board block diagram



Title		
MAIN		
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Leitungen/Busse die noch an freie IO anschließen sind und auch beliebig getauscht werden dürfen!!!



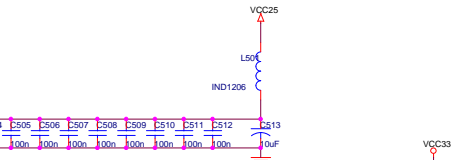
Leitungen/Busse die bereits an IOs angeschlossen sind und nicht getauscht werden dürfen!!!!

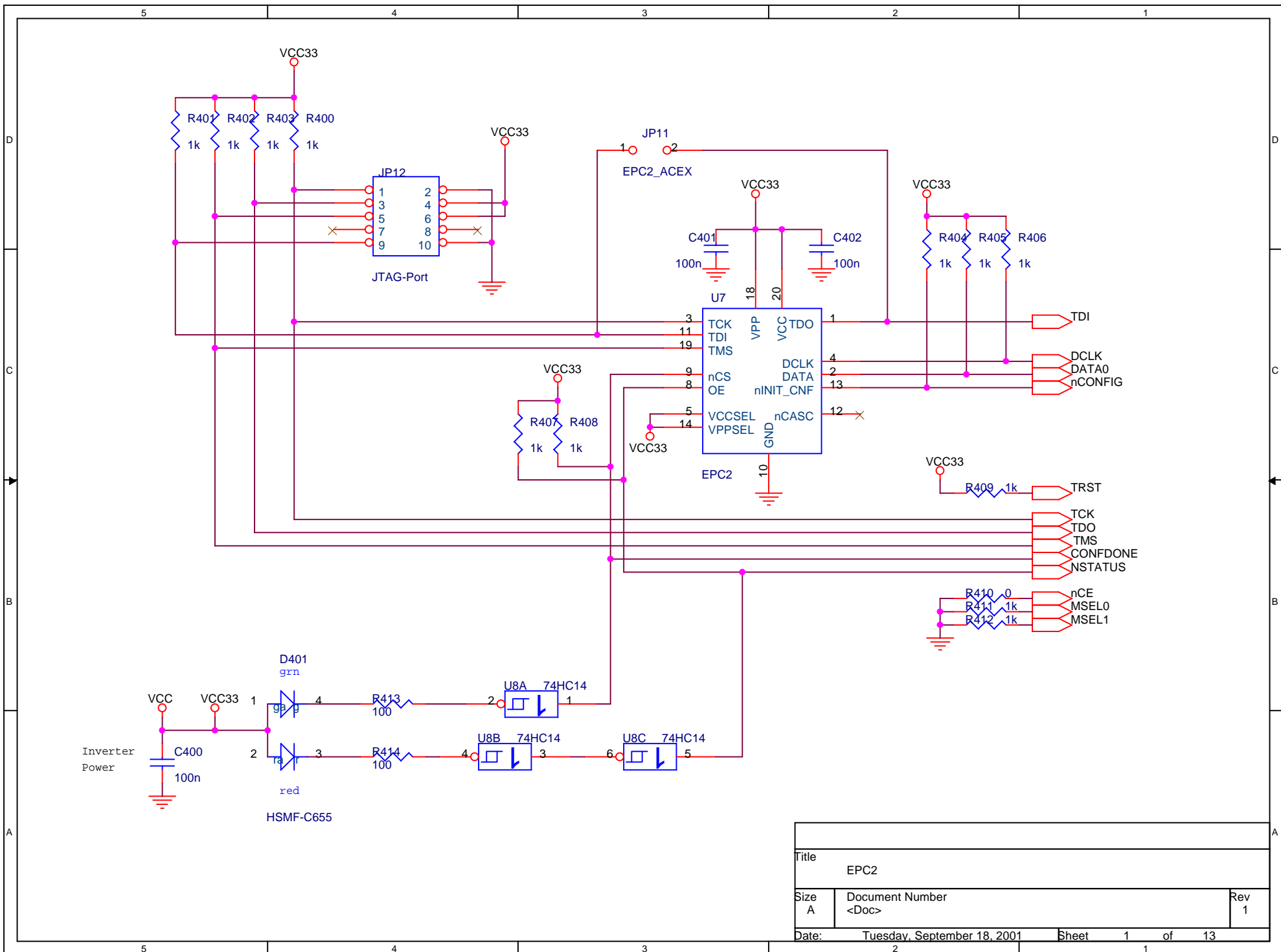


Nicht benutzbar, da zu dicht am PCI

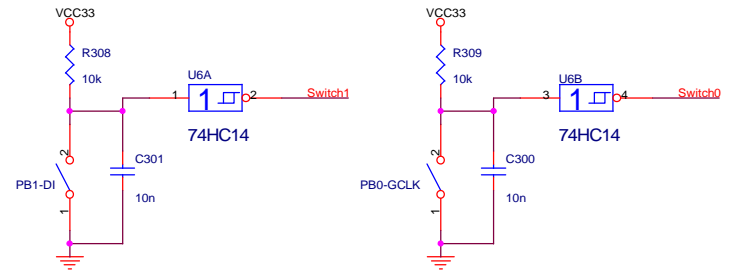
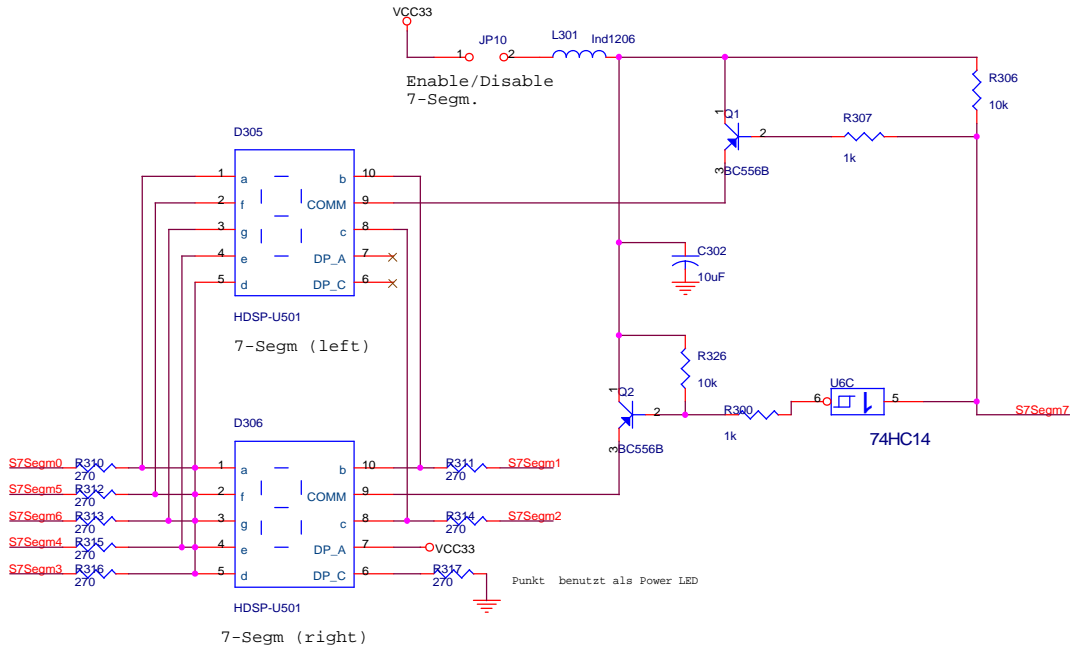
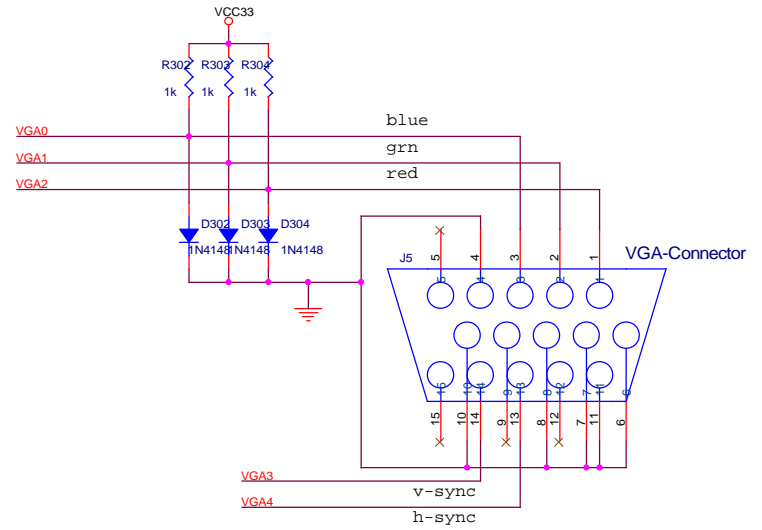
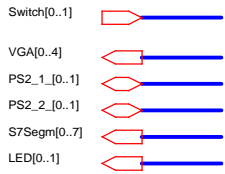
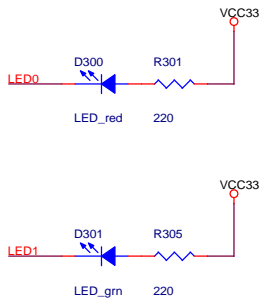
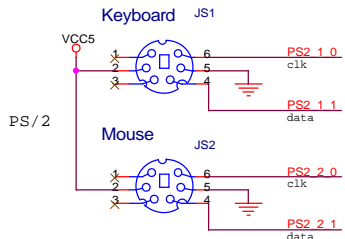


Clock wahlweise durch Oszillator oder über den PCI-Bus
Der Oszillator wird durch den FPGA umgeleitet, da sich der Global-CLK Pin zwangweise dicht am PCI-Bus befindet.
Es ist also OSC_CLK zur Zeit am Pin 182 am FPGA angeschlossen, und wird dann intern zu PIN71 verschaltet.

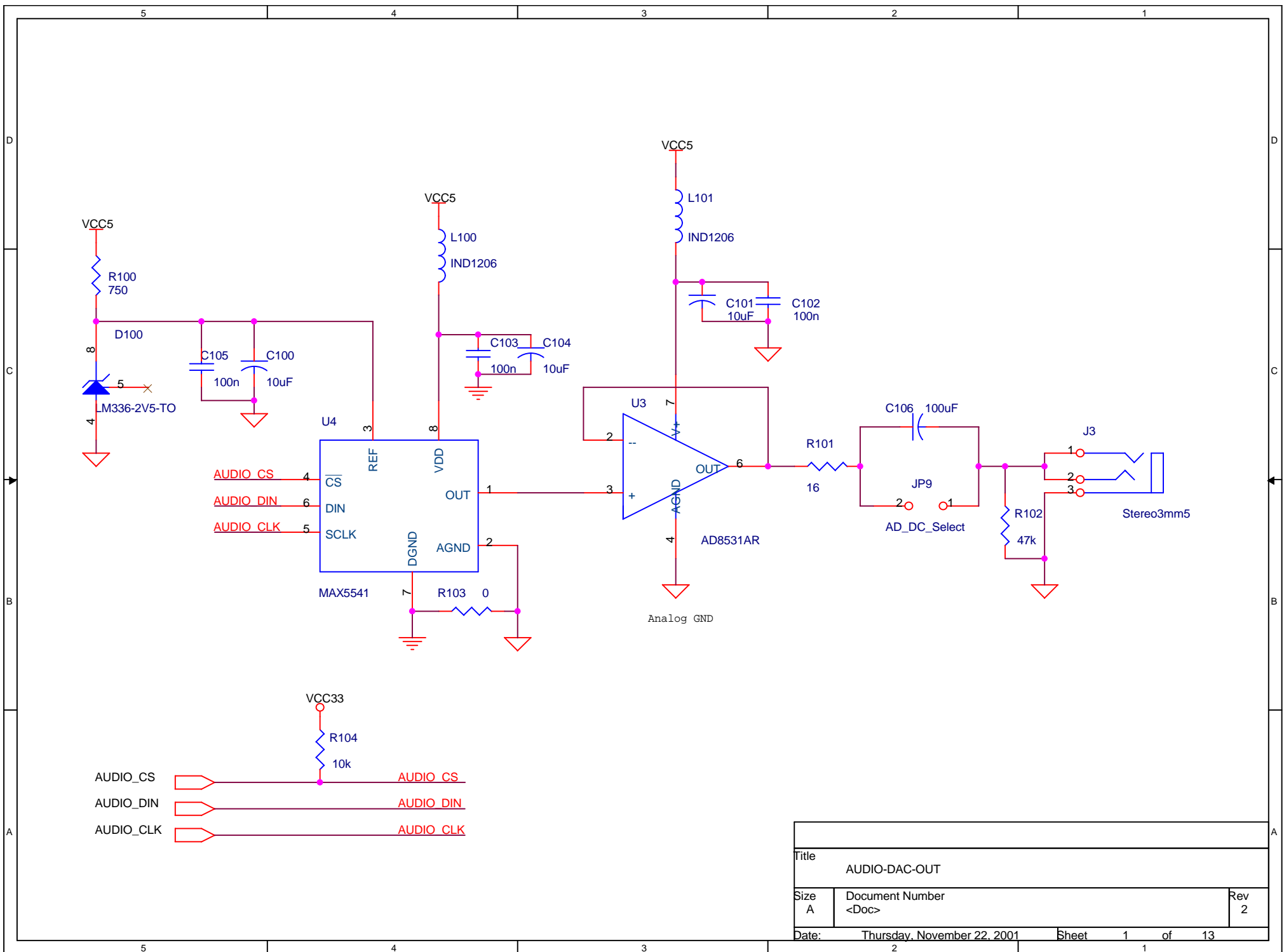




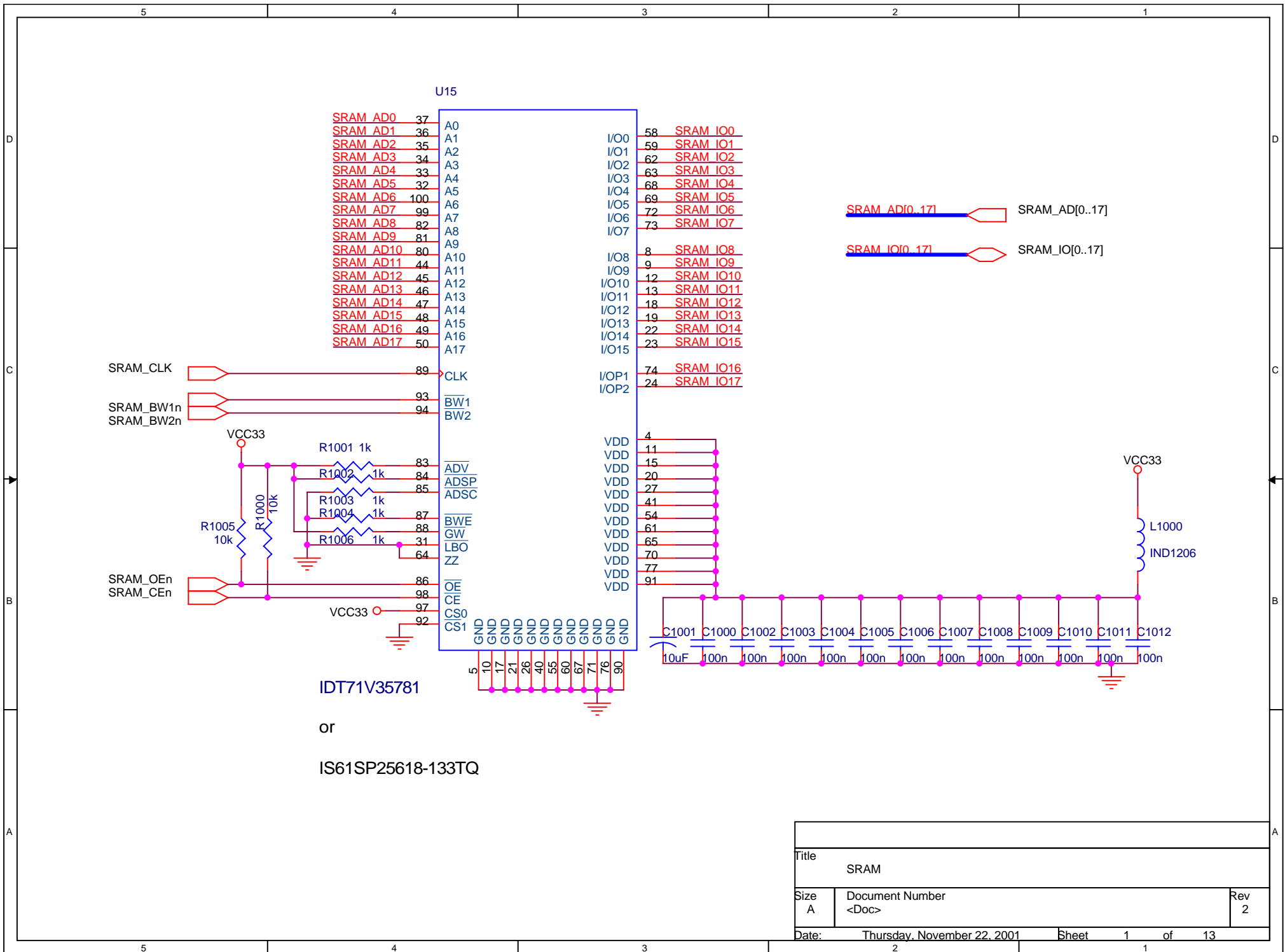
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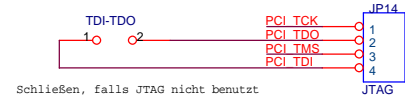
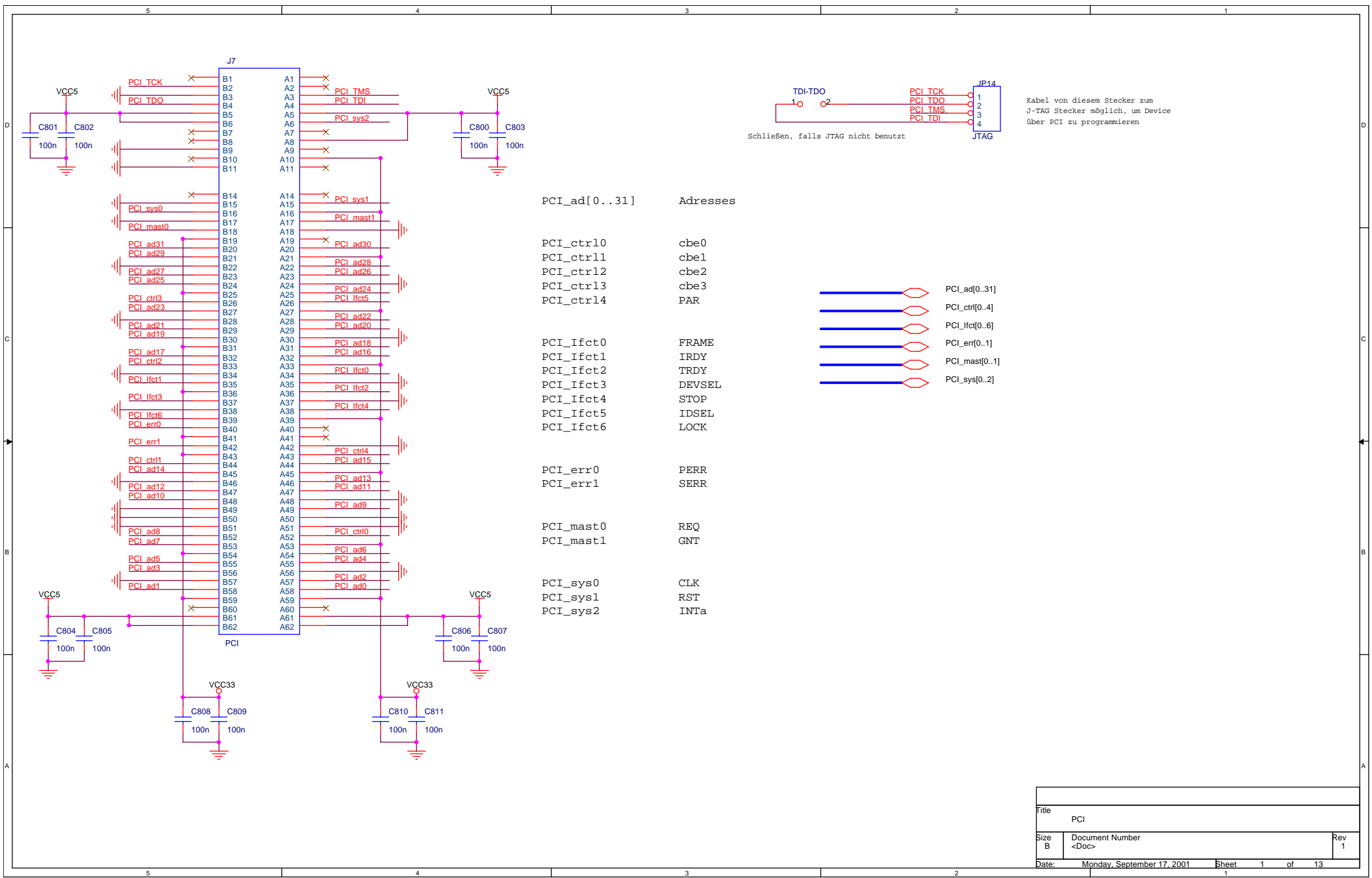
Title		
DIVERS		
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Title		
AUDIO-DAC-OUT		
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A	<Doc>	2
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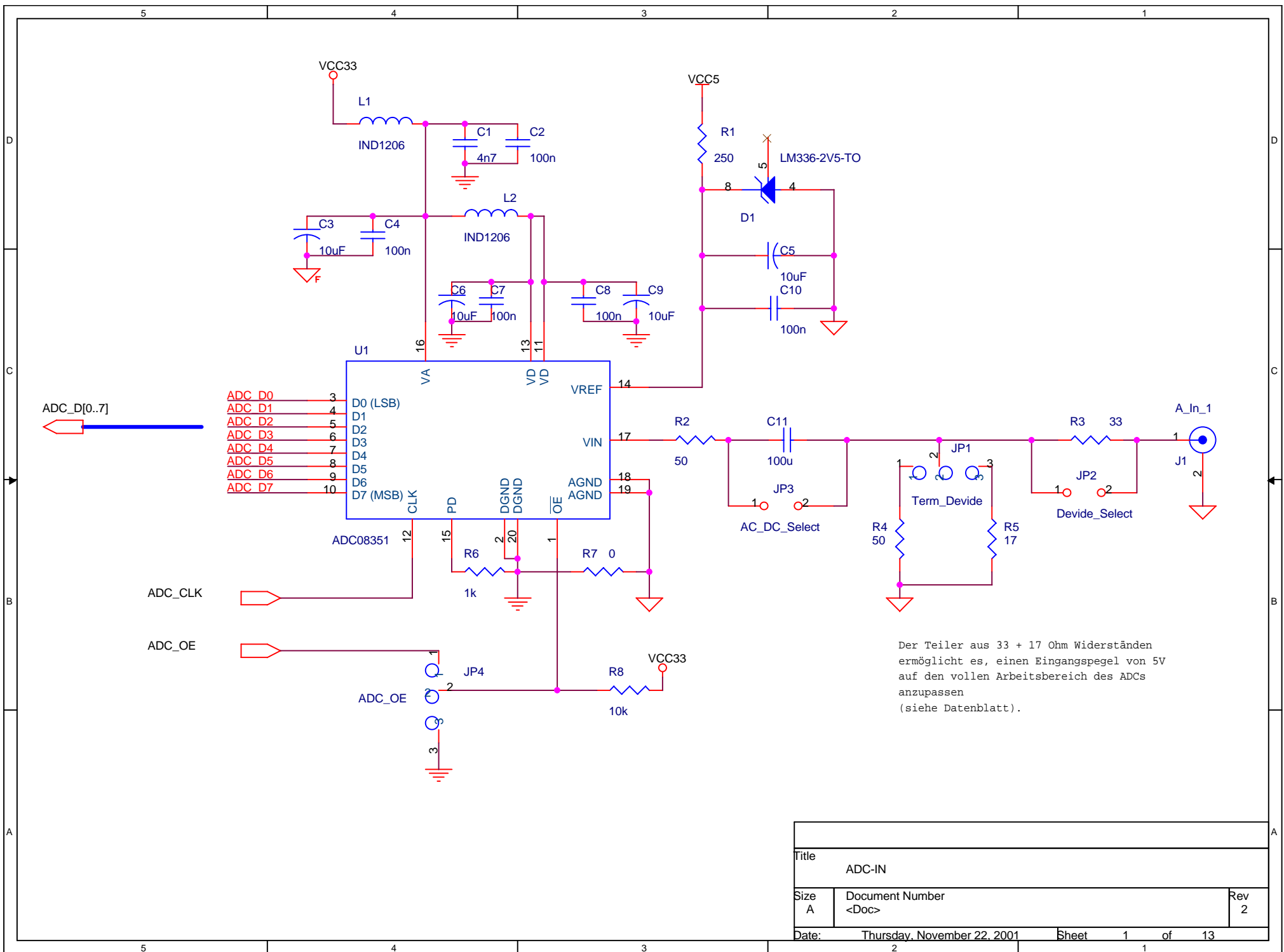


Title		
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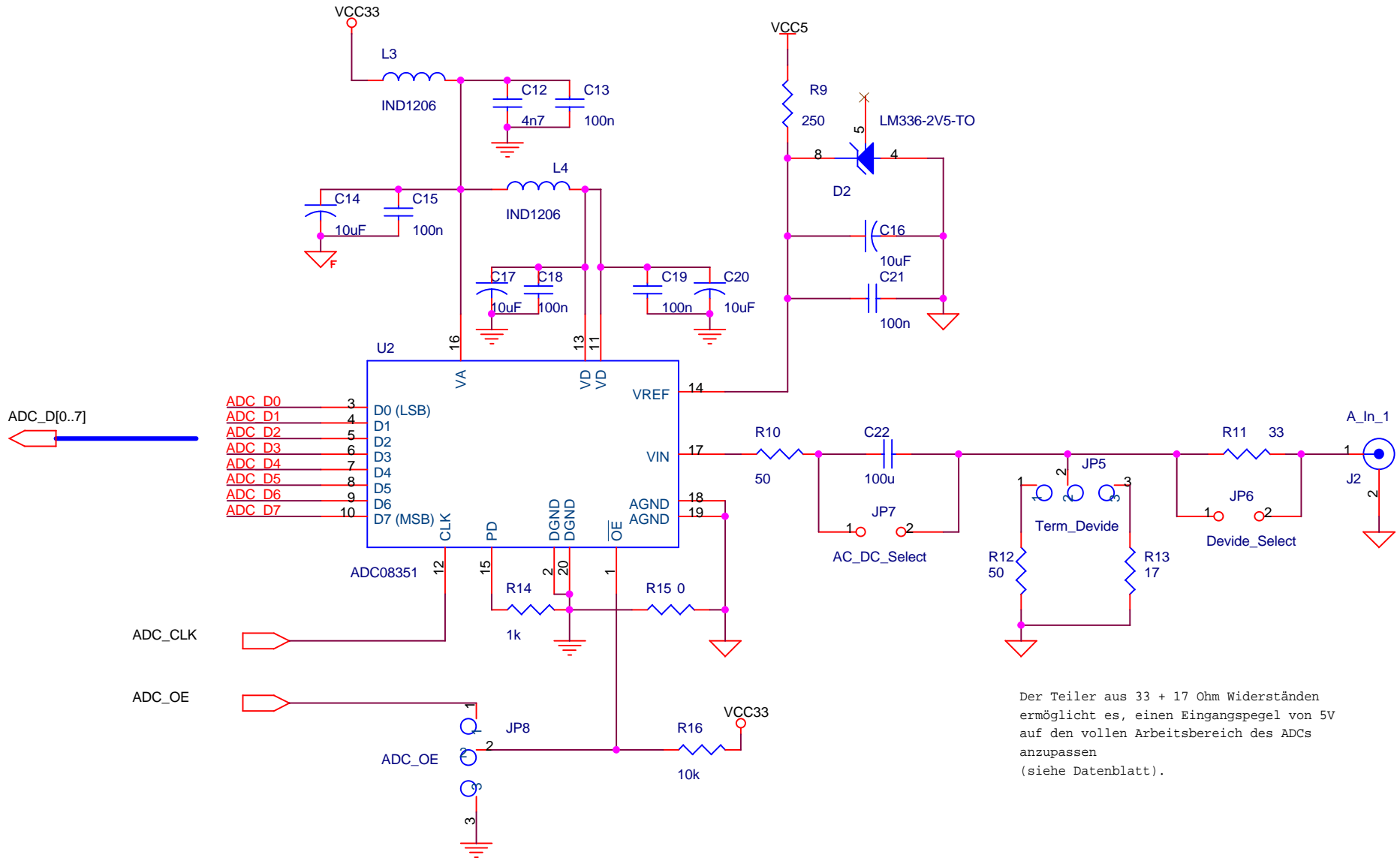


Kabel von diesem Stecker zum J-TAG Stecker möglich, um Device über PCI zu programmieren

Title		
PCI		
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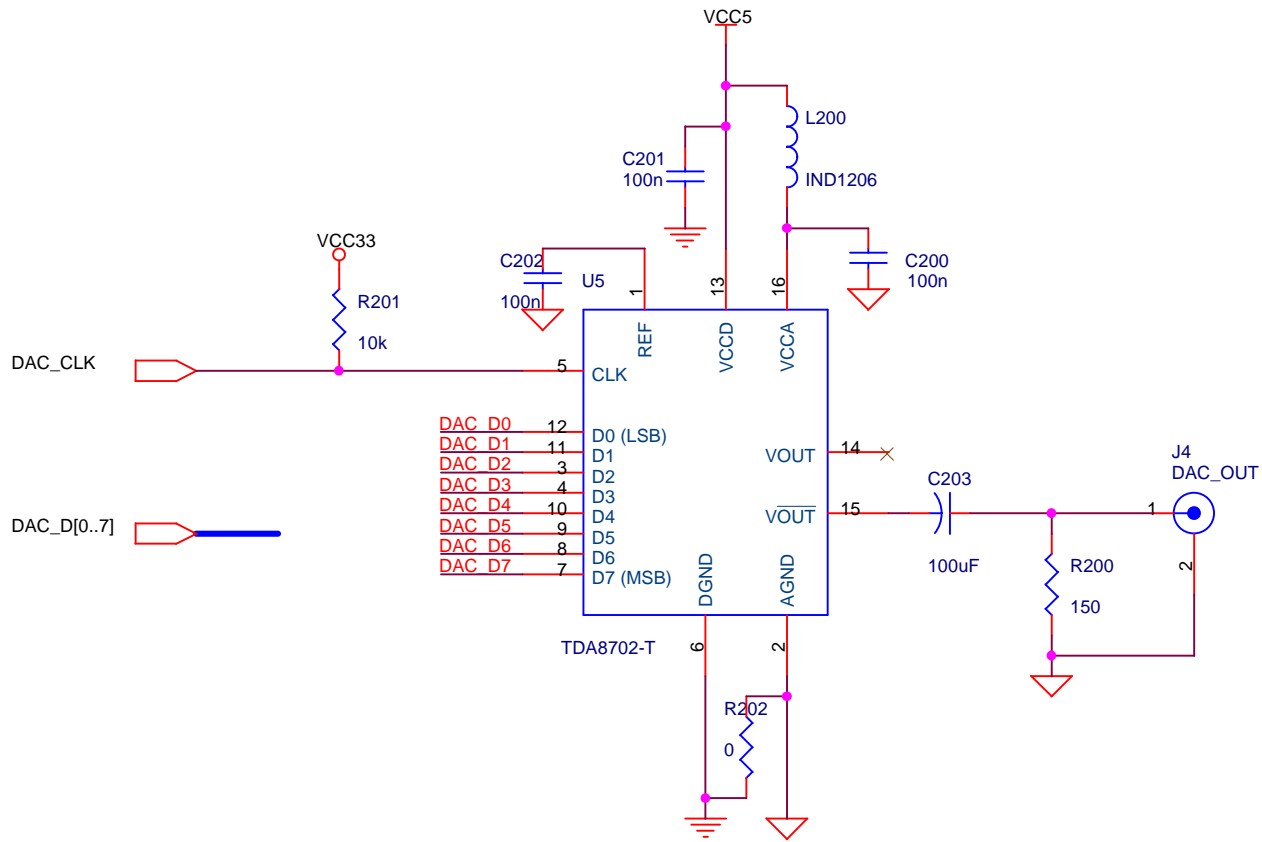
Title		
ADC-IN		
Size	Document Number	Rev
A	<Doc>	2
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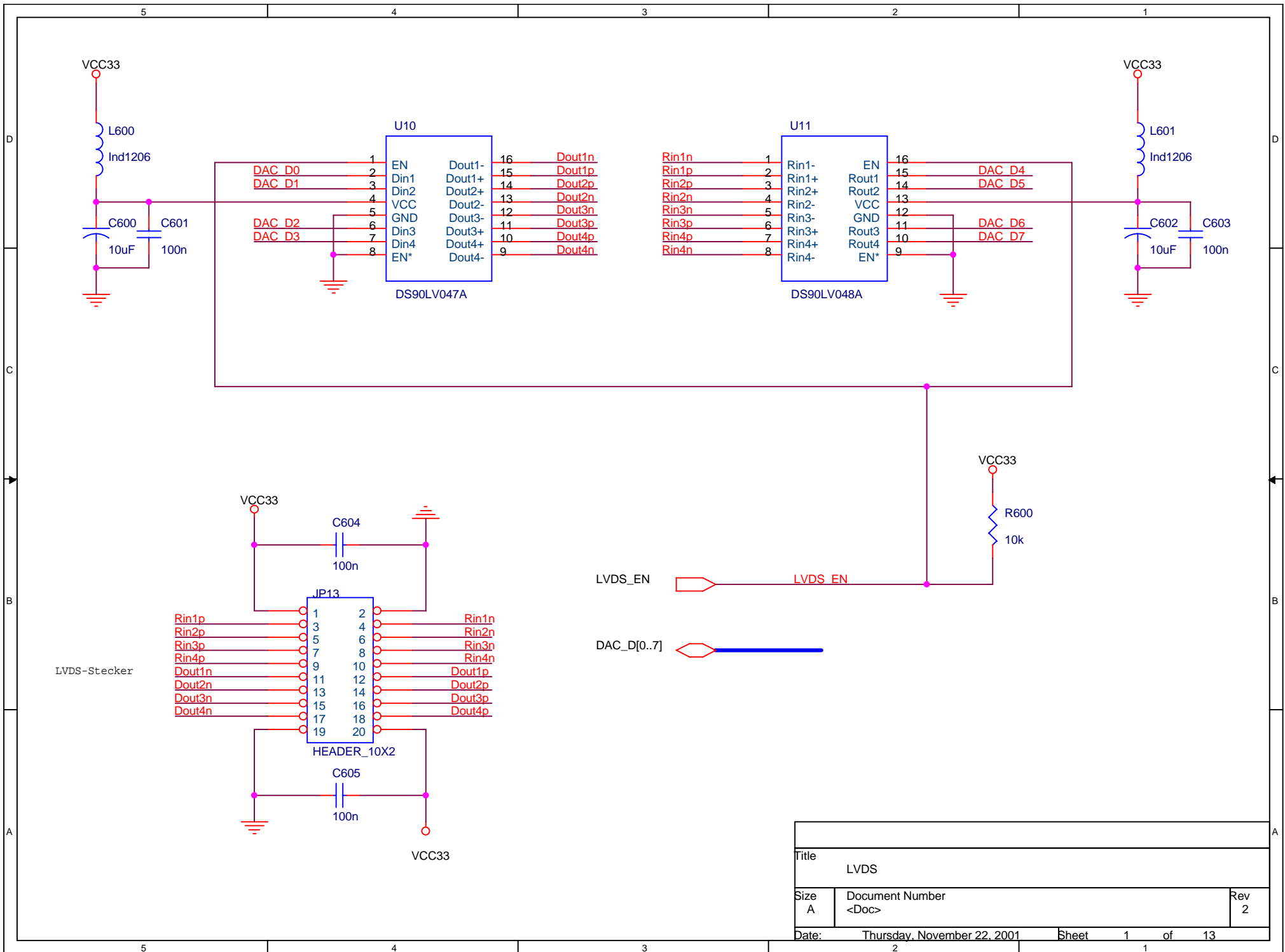
- ADC_D0 3
- ADC_D1 4
- ADC_D2 5
- ADC_D3 6
- ADC_D4 7
- ADC_D5 8
- ADC_D6 9
- ADC_D7 10

Der Teiler aus 33 + 17 Ohm Widerständen ermöglicht es, einen Eingangspegel von 5V auf den vollen Arbeitsbereich des ADCs anzupassen (siehe Datenblatt).

Title		
ADC-IN		
Size	Document Number	Rev
A	<Doc>	2
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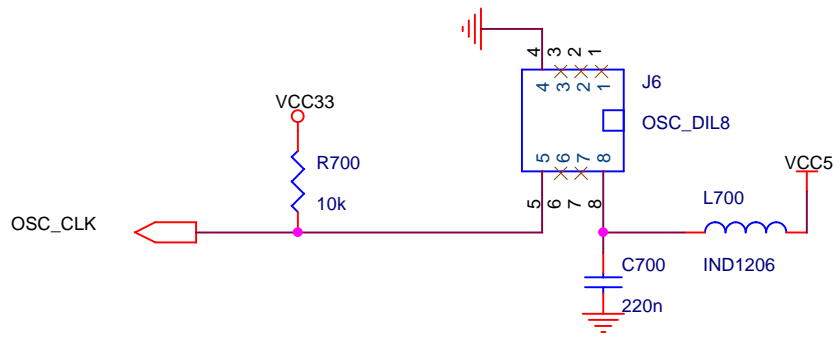


Title		
DAC-OUT		
Size	Document Number	Rev
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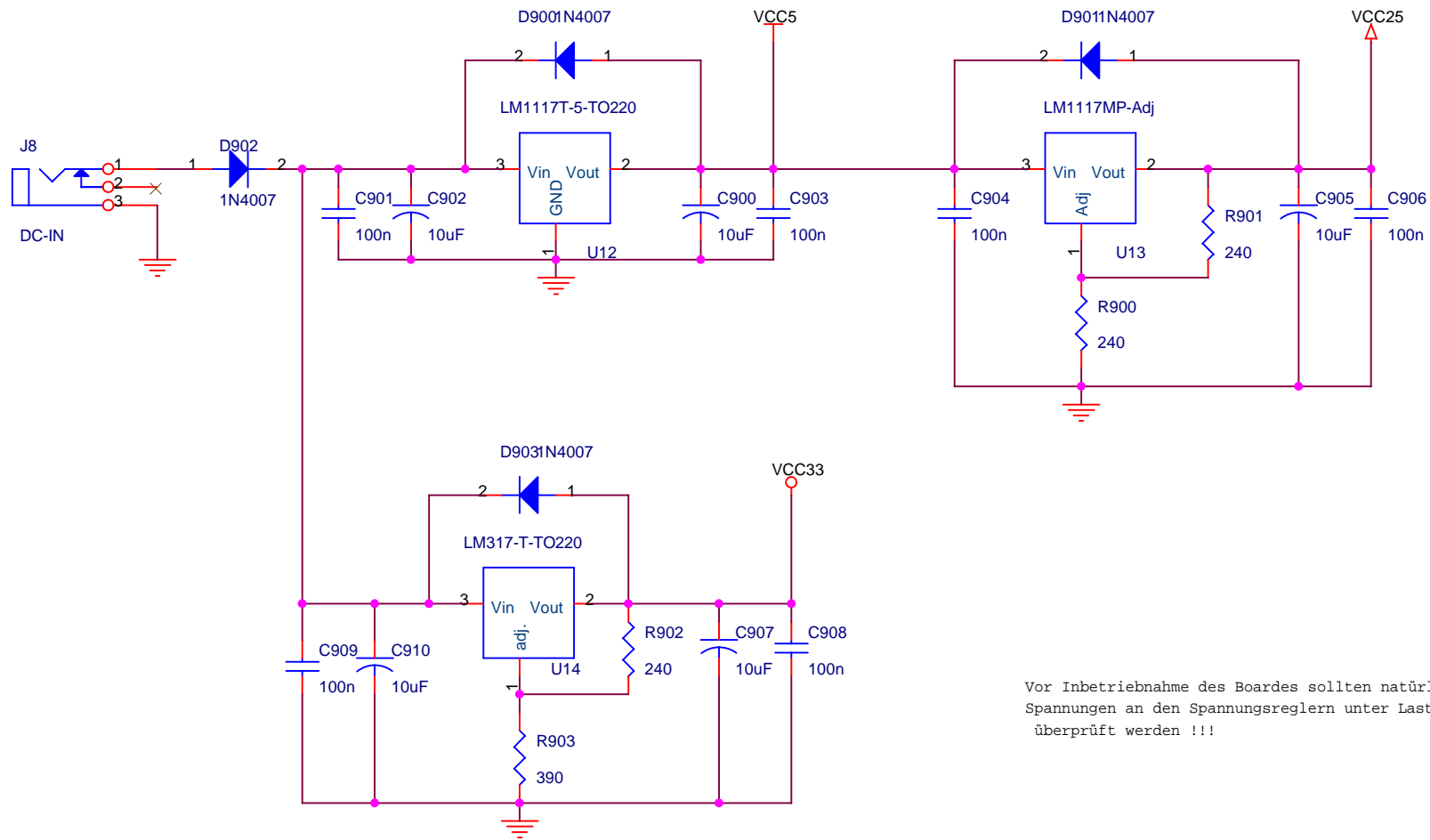


LVDS-Stecker

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LVDS		
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Title		
OSC		
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Vor Inbetriebnahme des Boardes sollten natürlich die Spannungen an den Spannungsreglern unter Last überprüft werden !!!

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POWER		
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