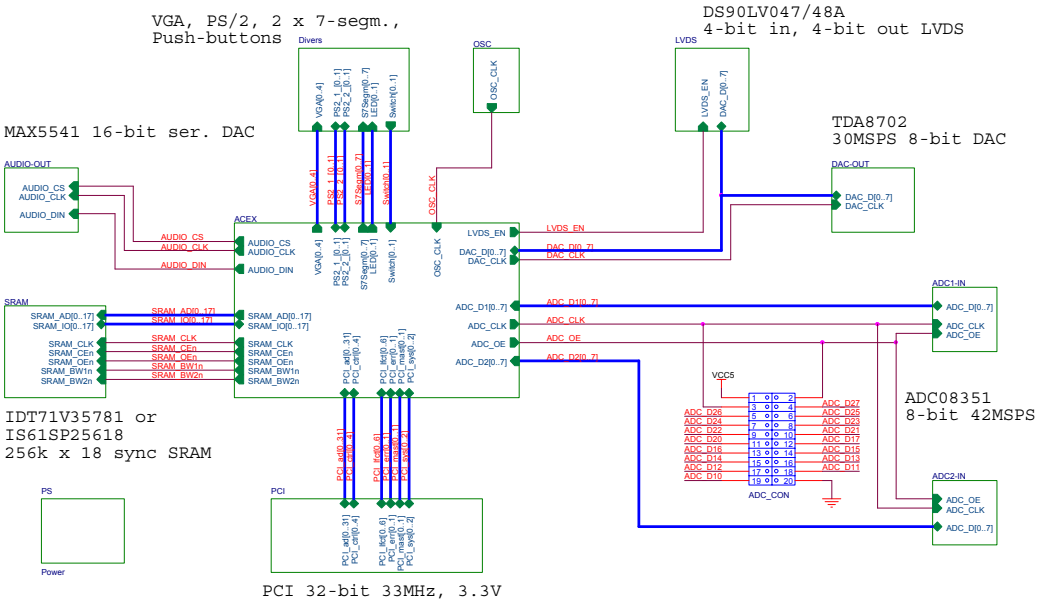
The KIP ACEX Board – A Short Description

The ACEX Board was designed to meet the needs for:

1) Education – learning digital electronics and computer architecture;
2) Prototyping and testing of digital cores before instantiating them in ASICs;
3) Data acquisition with PCs in lab experiments.



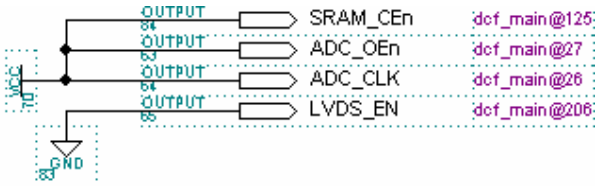
We have selected the ACEX Family because it is cheap, has enough sophisticated internal structure (PLLs, multifunctional memory blocks - EAB) and it is supported by the free development tool MAX+PLUS II of Altera. The surrounding chips allow implementing not only pure digital designs using PCI, SRAM, VGA, LVDS, but also mixed designs using ADCs and DACs.

The resources on board are:

CPLD – Altera ACEX	EP1K30|50|100 QC208-1|2|3 (any combinations)
SSRAM – 256k x 18	IDT71V35781 (IDT) or IS61SP25618 (ISSI)
LVDS – 4 in, 4 out	DS90LV047/48A (NSC)
Quartz oscillator	any standard type in DIL8 package (e.g. 50 MHz)
30MSPS 8-bit DAC	TDA8702 (PHILIPS)
2 x 8-bit 42MSPS ADCs	2 x ADC08351 (NSC)
16-bit ser. DAC	MAX5541 (MAXIM)
Connectors:	3 x analog (DAC+2xADC), headphone, DC power in (7.5V), PCI, 2 x PS/2, 1 x VGA, 1 x Header 2x10 with pinout for logic analyzer Termination Adaptor HP 01650-90920
Others	2 push buttons, 2 x 7 segment indicators, 2 x LEDs
ACEX Configurations	JTAG (using Altera ByteBlasterMV) or EPC2LC20

Further information:

The ***table with the pins*** of the ACEX is stored in the .acf file format for MAX+PLUS II in the file ALL_PINS.ACF. The user should ***put some pins to proper constants***, in order to avoid memory, LVDS receiver and ADCs to drive active although not used in the design.

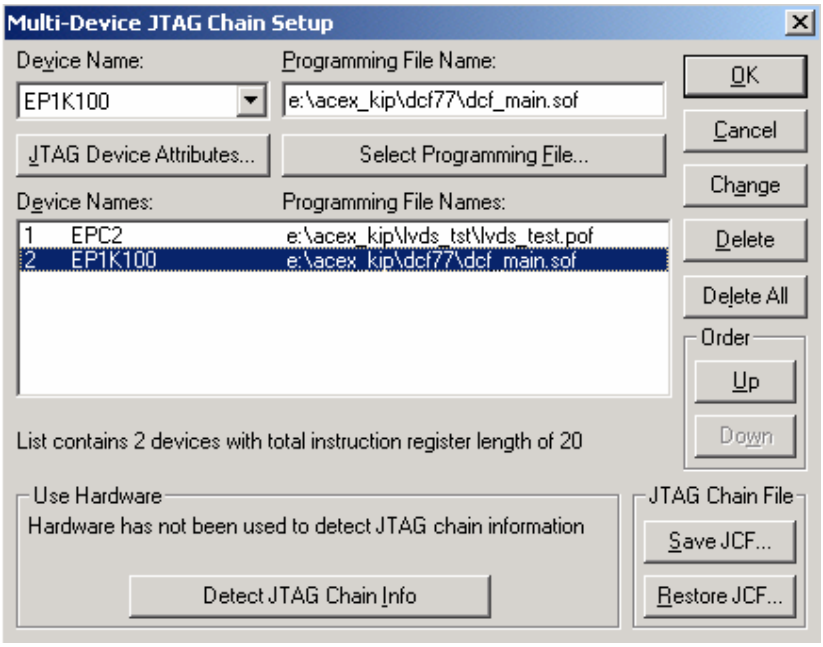


The ***complete schematic*** of the board with the component layout can be found in PDF format in acx_board_sch.pdf.

The user is advised to read the ***data sheets*** of all components on board that will be used in the design.

Configuration:

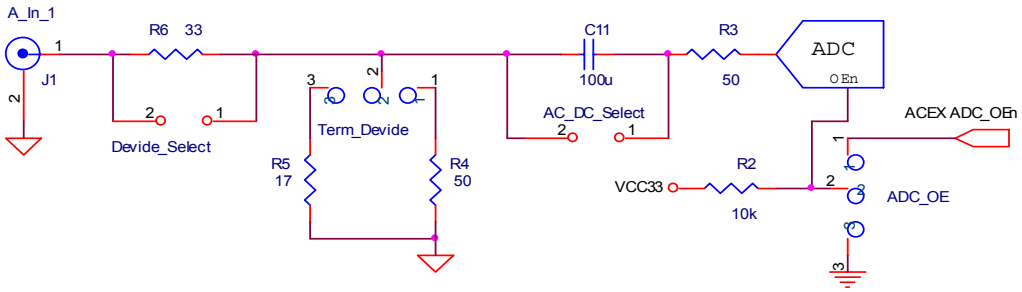
1) If the EPC2 chip is not installed in the socket, then the jumper JP11 should be closed. In this case it is not necessary to define a JTAG chain in the Programmer of MAX+PLUS II, it is enough to click on the Configure button.
2) If the EPC2 chip is plugged into the socket, then the jumper JP11 should be left open. In this case it is necessary do define a JTAG chain in the Programmer, and then add the programming files in the proper order.

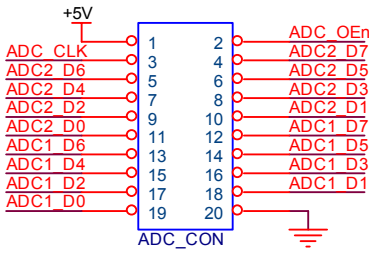


The configurations status can be monitored using the red/green LED near the EPC2: red is on when CONFIG_DONE is high, the red is on when nSTATUS is low.

Using the flash-ADCs:

Each ADC has its own jumpers for selecting the termination and attenuation of the input signal, as well as for setting the output enable to permanently enable/disable or control through the ACEX design.



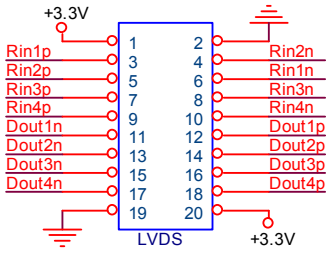


It is possible to use some or all of the ADC signals as LVTTL in/out. They are available on the header right to the ADCs. In such a case the user should disable the corresponding ADC outputs.
The pinout of the connector is the same as by the HP logic analyzer termination adapter and is shown here. It is even possible to supply the board through this connector.

Using the fast DAC:

The 8 data bits of the fast DAC are shared with the LVDS receiver/driver. If the LVDS will be not used the LVDS_EN signal should be put permanently to low (disable). Otherwise it is possible to control the LVDS_EN signal and use bidirectional pins for LVDS_in[3..0].

Using the LVDS:



In order to use the LVDS receiver and driver the signal LVDS_EN should be high. If the receiver is the only one (no multidrop) then it is necessary to solder termination resistors (normally 100 Ohm SMD 0805 or 0603) directly between the pins of the connector on the solder side. In case of a multidrop connection, the termination resistors should be soldered only on the last board.

Using PS/2 mouse/keyboard, VGA:

There are two standard PS/2 connectors and a VGA (15pin) connector. In order to use the keyboard, mouse and VGA output in the designs it is recommended to get the design files of the book “Rapid prototyping of digital systems”, by James O. Hamblen and Michael D. Furman.

Using the two digit 7-segment indicator and the LEDs:

The output to the two 7-segment displays must be multiplexed in time using the signal R7S_mux at a frequency about 100Hz. R7S[1..7] are the a,b,c,d,e,f,g-segments. The power to the indicators can be switched off by removing the jumper JP10. The ACEX pins must be tied low in order to switch the LEDs on. The same is applicable for the two single LEDs (LED_GRN and LED_RED).

Using the push-buttons:

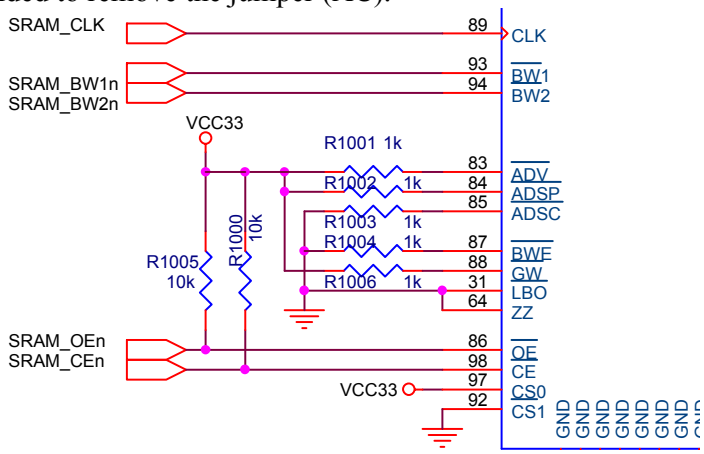
The two push button signals pass first through inverting Schmidt-trigger (74HC14) stages and then come to the ACEX active high. Nevertheless a debouncing circuit should be used to avoid multiple pulses OR larger capacitors should be soldered (C300/308) to increase the time-constant.

Using the serial DAC and the headphone output:

Here it is recommended to read the data sheet of the MAX5541. Shortly, the MSB is shifted first, LSB last, the data bit (AUDIO_DAT) is stored at the rising edge of the serial clock (AUDIO_CLK), the strobe/CSn (AUDIO_CSn) must be low during the shift and must be pulsed high at the end. There is a jumper at the output to select between direct output (DC) or capacitor coupled output (AC). For headphone operation it is recommended to remove the jumper (AC).

Using the synchronous static RAM:

Here it is strongly recommended to read the data sheets in order to use it correctly and to avoid bus conflicts. Not all control pins of the SSRAM are available to the ACEX, see the schematic to the right.



PCI:

ACEX 1K are not tolerant to 5V PCI signals, therefore the board is designed for 3.3 V PCI. For PCI designs a PCI-core (32 bit) will be necessary (see the Altera web-page).

Power supply:

There are voltage regulators on board, so the board can be used as stand alone, not only in PC as PCI board. The voltage connector is standard type, the positive pin is in the middle, ground is outside. There is a diode serially to the input, so connecting power with false polarity will not destroy the board. The minimal input voltage is about 7.5V. If the voltage regulators are very hot, small radiators can be mounted. The I/O cells of the ACEX are powered by 3.3V. The configuration device pull-ups should not be used, there are pull-ups on the board.

Test & reference designs, some ***modules (SPI, CPU)*** and ***additional information*** are available upon request. Contact: Prof. Dr. Volker Lindenstruth, Dr. Venelin Angelov, Kirchhoff Institute for Physics, University of Heidelberg, Germany.
www.kip.uni-heidelberg.de/ti

