Beetle1.1 – First Results

Beetle1.1 arrived in Heidelberg on June 26 2001 (22 dies)

First Results:

- chip is programmable via I2C−Interface
- all chip registers can be read back via I2C−Interface
- all readout modes (i.e. 4x (32:1), 2x (64:1), 1x (128:1)) work
  (Pipeline Column Number (PCN) is correctly encoded and has the right levels)
- control logic works:
  - WriteMon/TrigMon circulate according to the programmed latency
  - a trigger reduces the cycle time of WriteMon and TrigMon by 1
  - after 16 consecutive triggers FifoFull gets active
- internal Testpulse−Generator works

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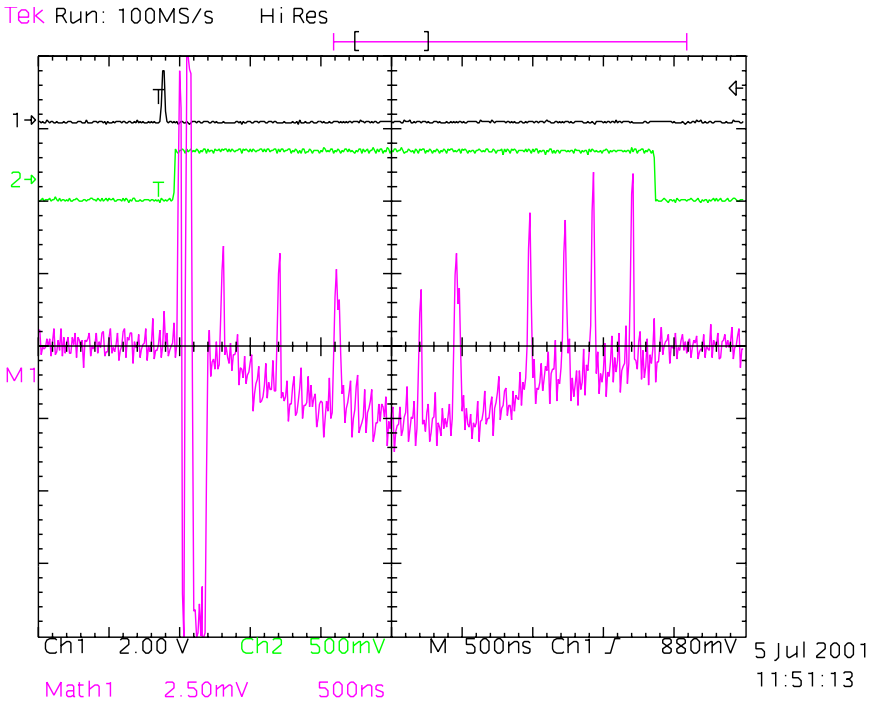
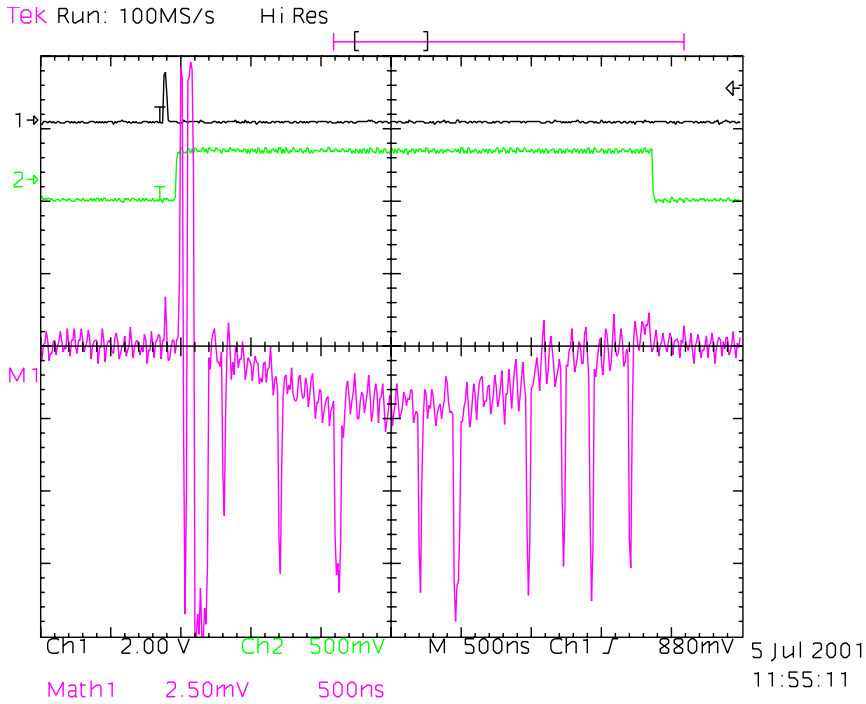
Analog Readout: 128 Channels on 1 Port

Input signal corresponding to 24.000 el. is coupled into 11 channels

(Channel No.: 4, 20, 36, 37, 60, 70, 71, 91, 101, 109, 120)





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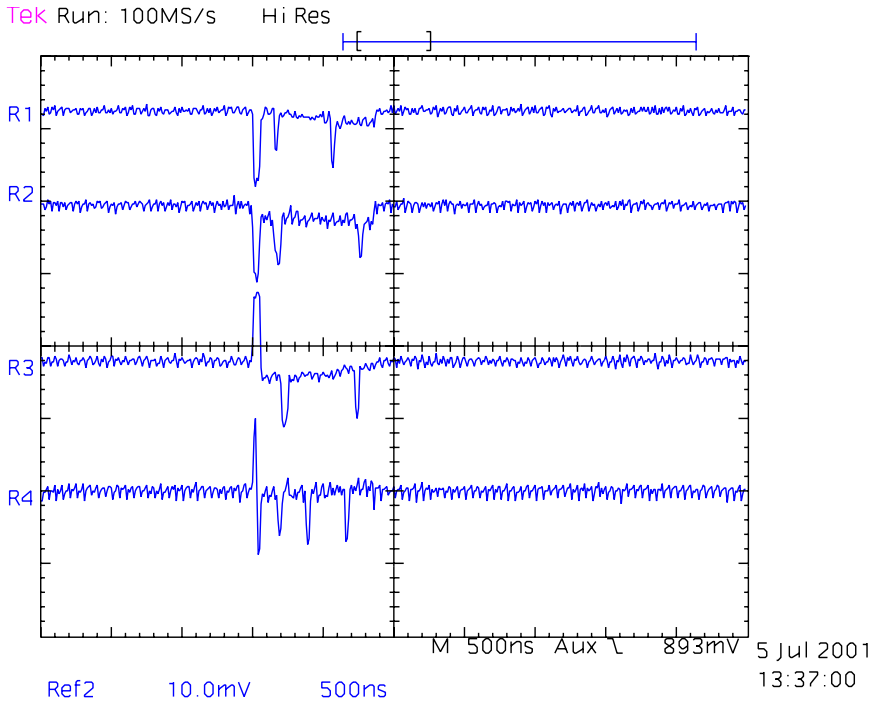
Analog Readout: 128 Channels on 4 Ports



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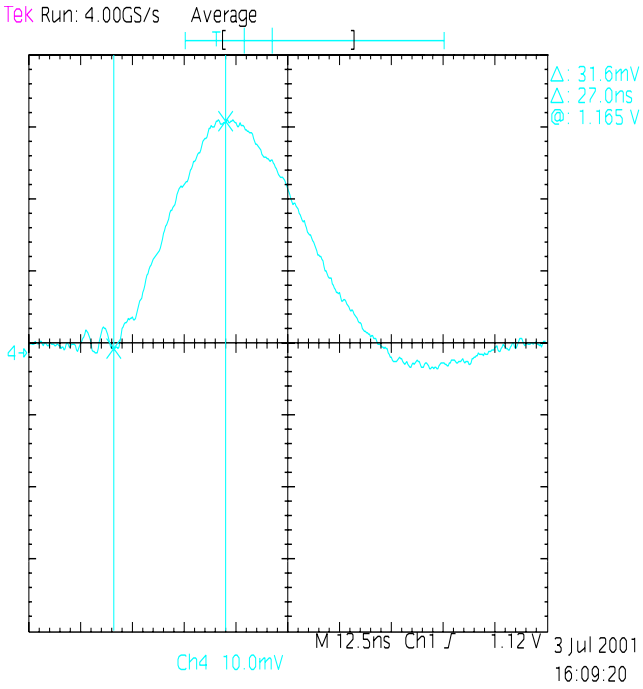
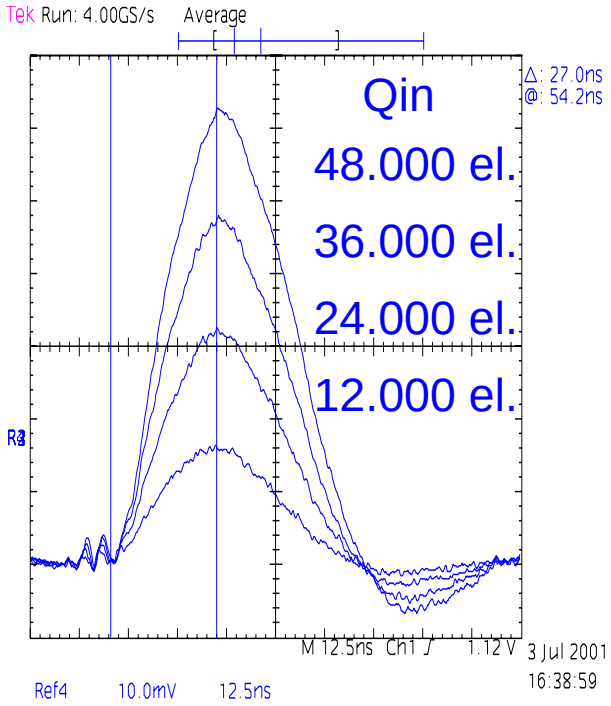
Frontend: Testchannel

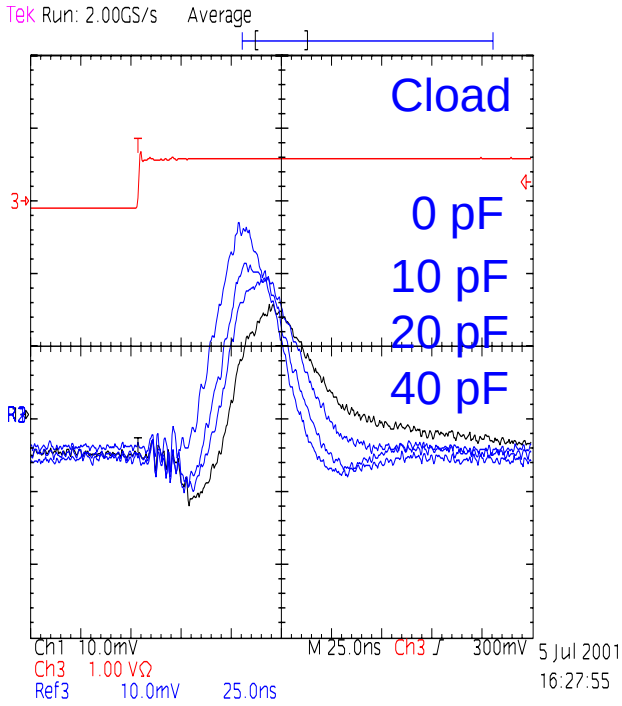
Cload = 0, Qin = 24.000 el.



Cload = 0



Qin = 24.000 el



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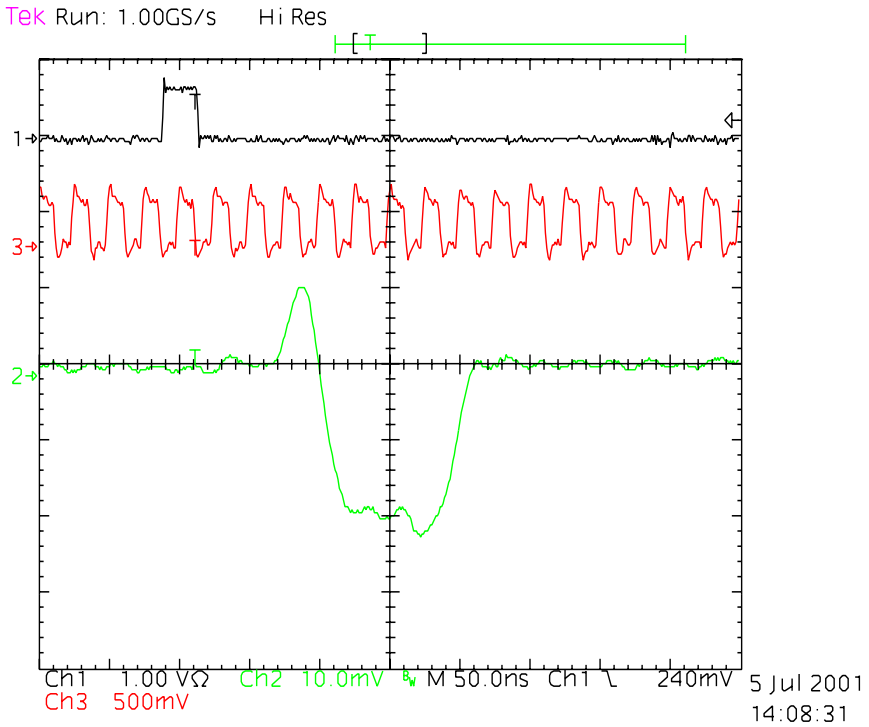
Pipeamp: Testchannel



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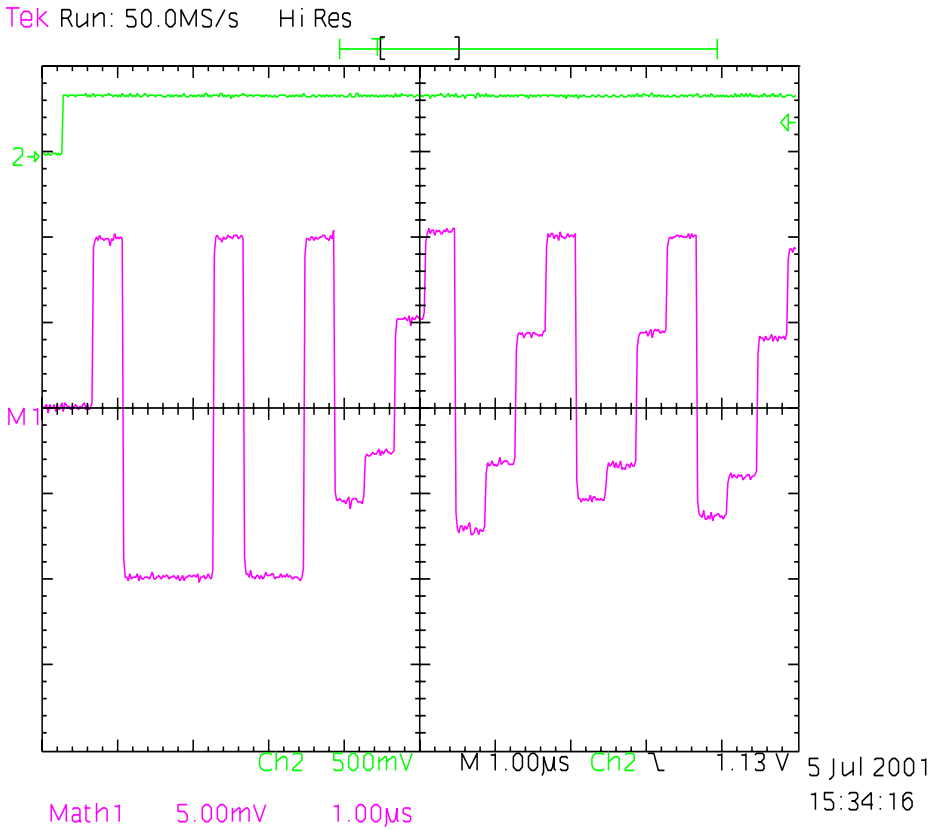
Internal Testpulse Generator



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