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Performance of the Beetle Readout Chip for LHCb

Niels van Bakel, Martin van Beuzekom, Eddy Jans, Sander Klous, Hans Verkooijen

(NIKHEF Amsterdam, Free University of Amsterdam)

Daniel Baumeister, Werner Hofmann, Karl-Tasso Knöpfle, Sven Löchner, Michael Schmelling

(Max-Planck-Institute for Nuclear Physics, Heidelberg)

Ulrich Trunk

(University of Heidelberg)

Neville Harnew, Nigel Smale

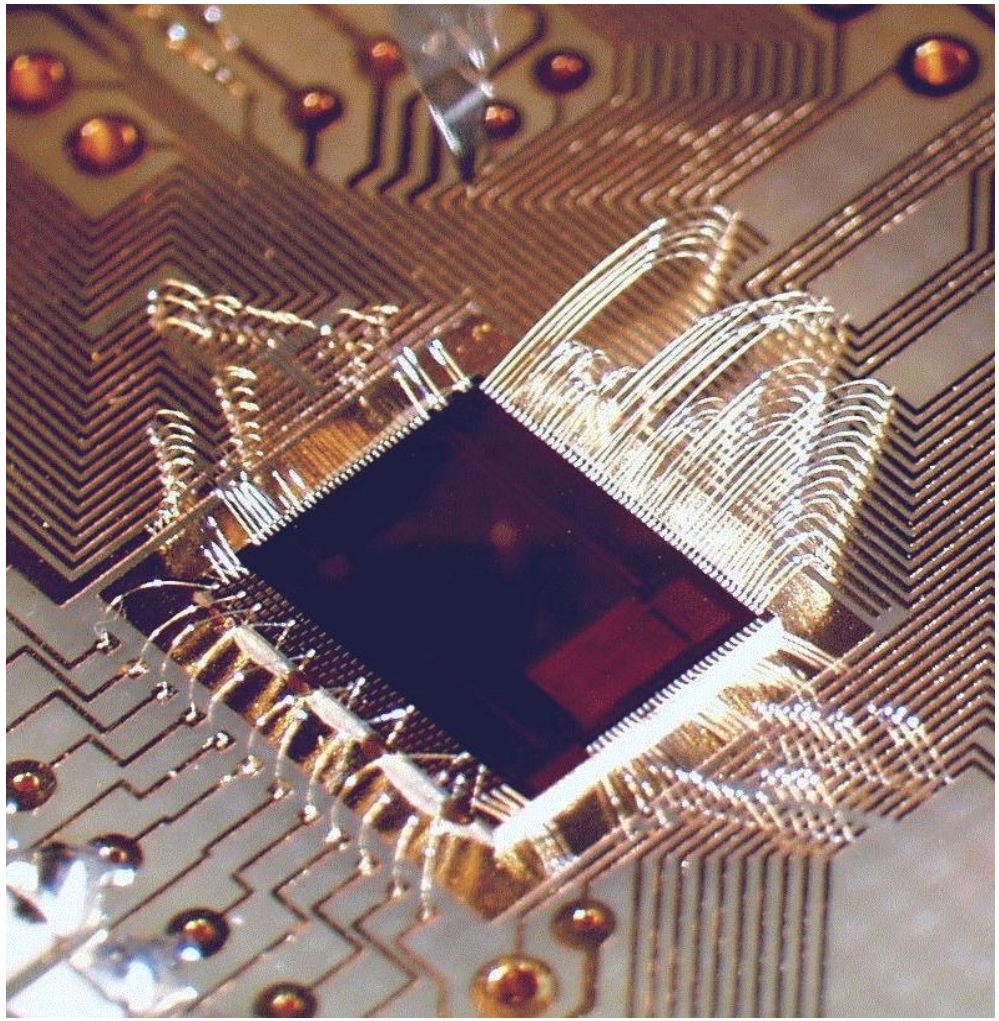
(University of Oxford)

Sven Löchner

ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Beetle: Outline

- Beetle Overview
- Beetle 1.2
  - Analogue readout
  - Front end
  - Comparator
  - Binary readout
  - Pipeamp / Multiplexer
  - SEU hard Fast Control / Slow Control
- Results from Total Ionizing Dose (TID) irradiation test
- Summary



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ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Beetle: A Readout Chip for LHCb

- analogue / binary pipeline chip
- providing a prompt binary readout for trigger applications
- integrated in a standard 0.25 µm CMOS technology
- designed for:
  - Silicon Vertex Detector
  - Pile-up Veto Trigger
  - Inner Tracker
  - RICH (in case of MAPMTs)

Key Specifications:

- 40 MHz sampling
- max. latency 4 µs
- 40/80 MHz readout
- fast shaping:
  - $t_{rise} \leq 25$ ns
  - remainder 25 ns after peak ≤ 30%
- accept up to 16 consecutive triggers
- readout time ≤ 900 ns / trigger
- radiation hard ≥ 10 Mrad

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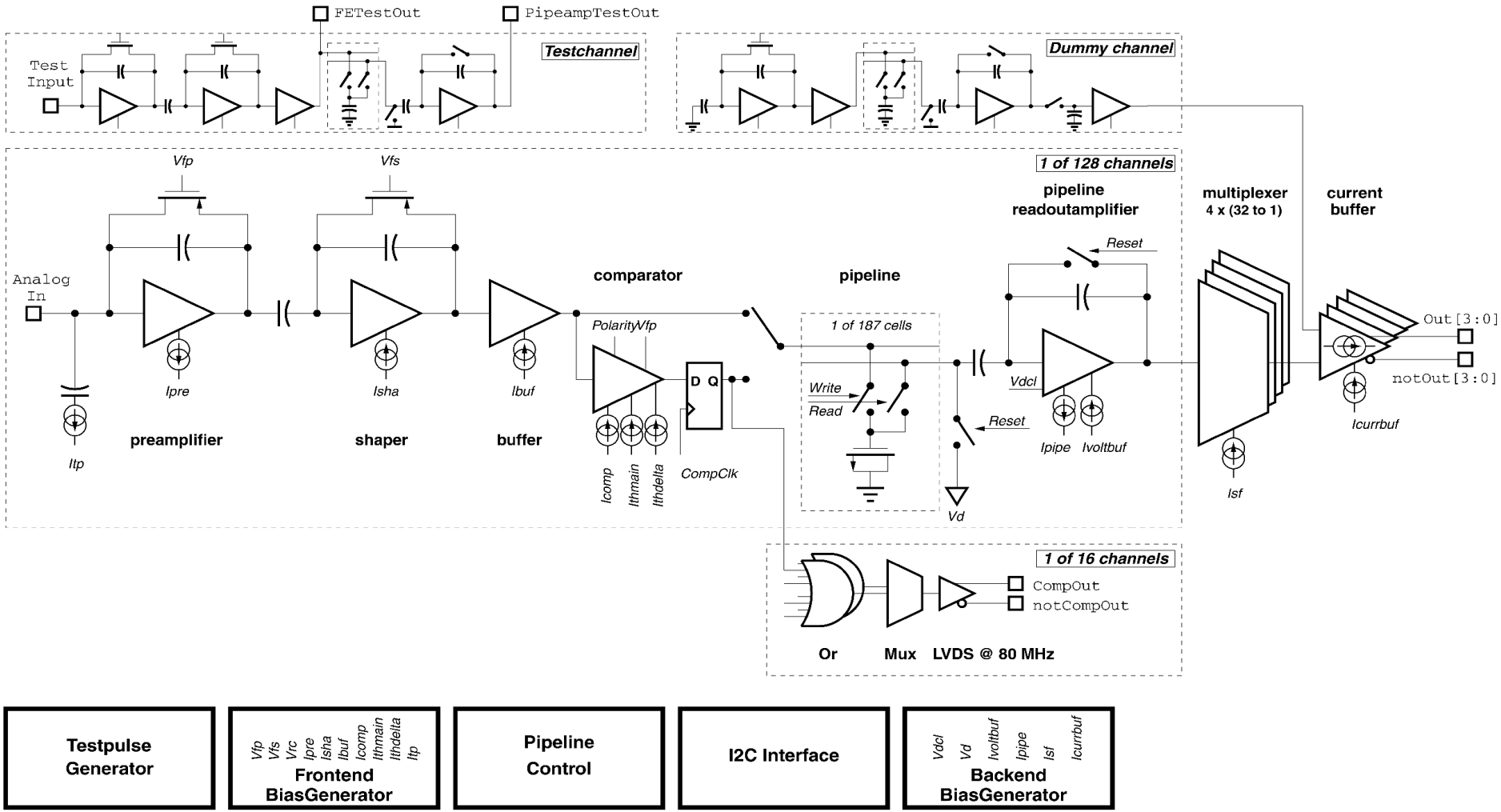
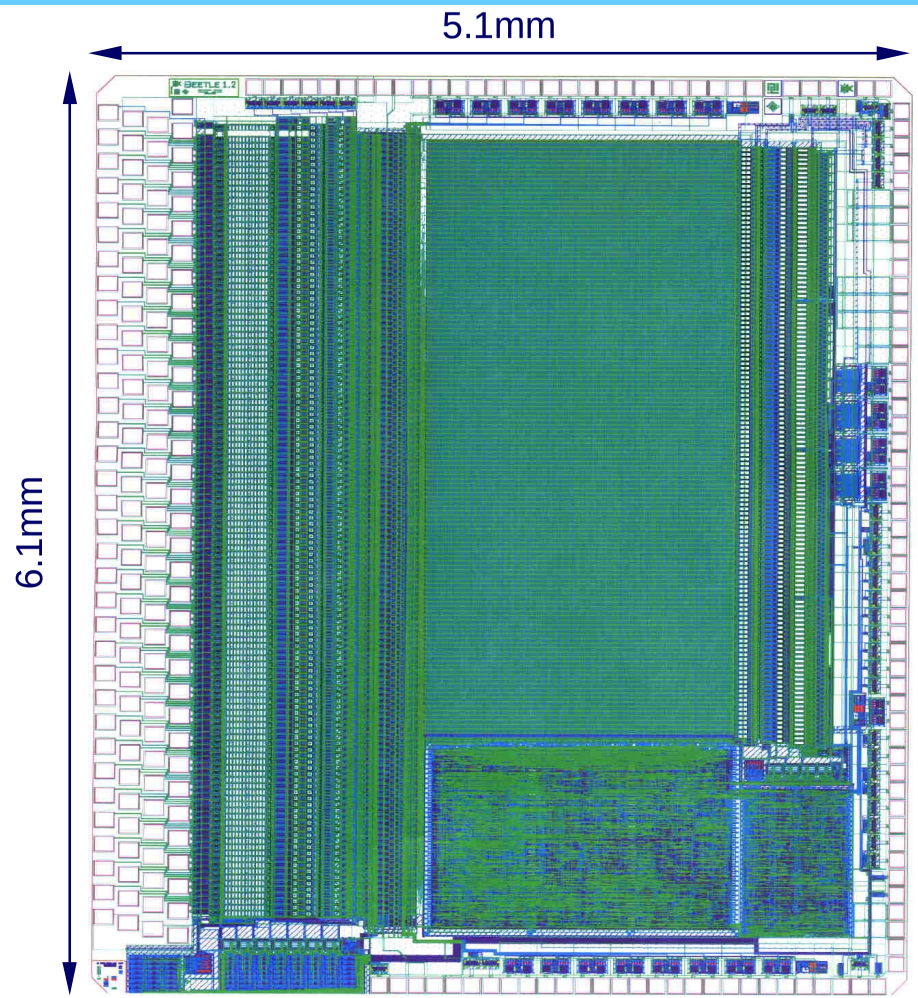
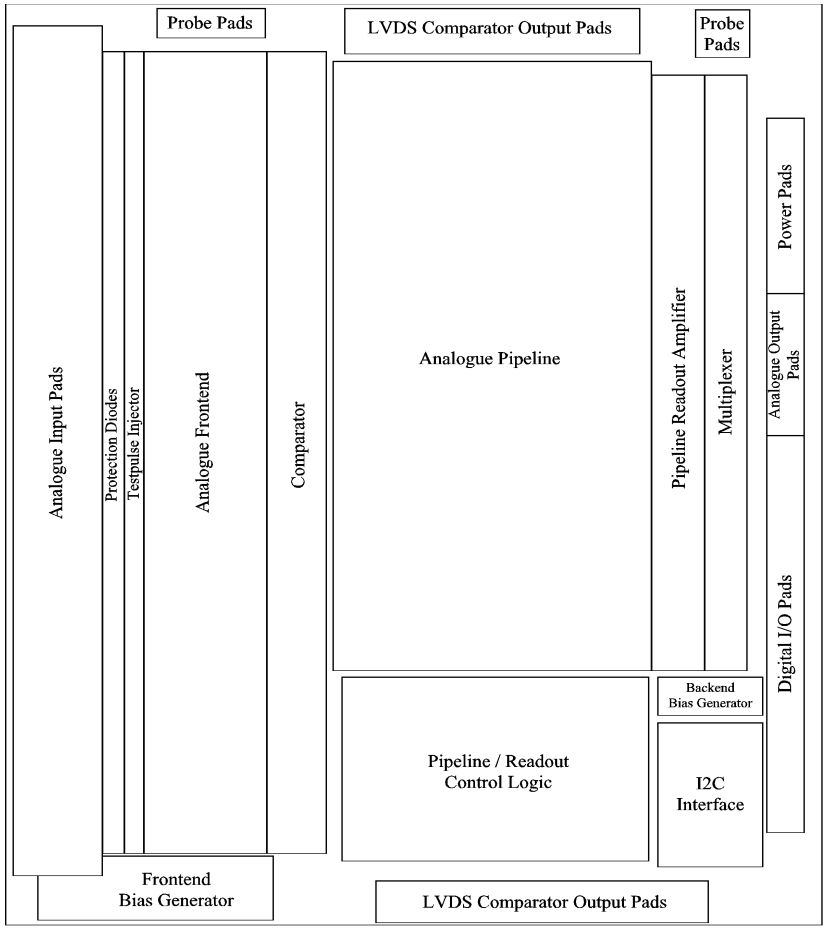
Beetle: Architecture



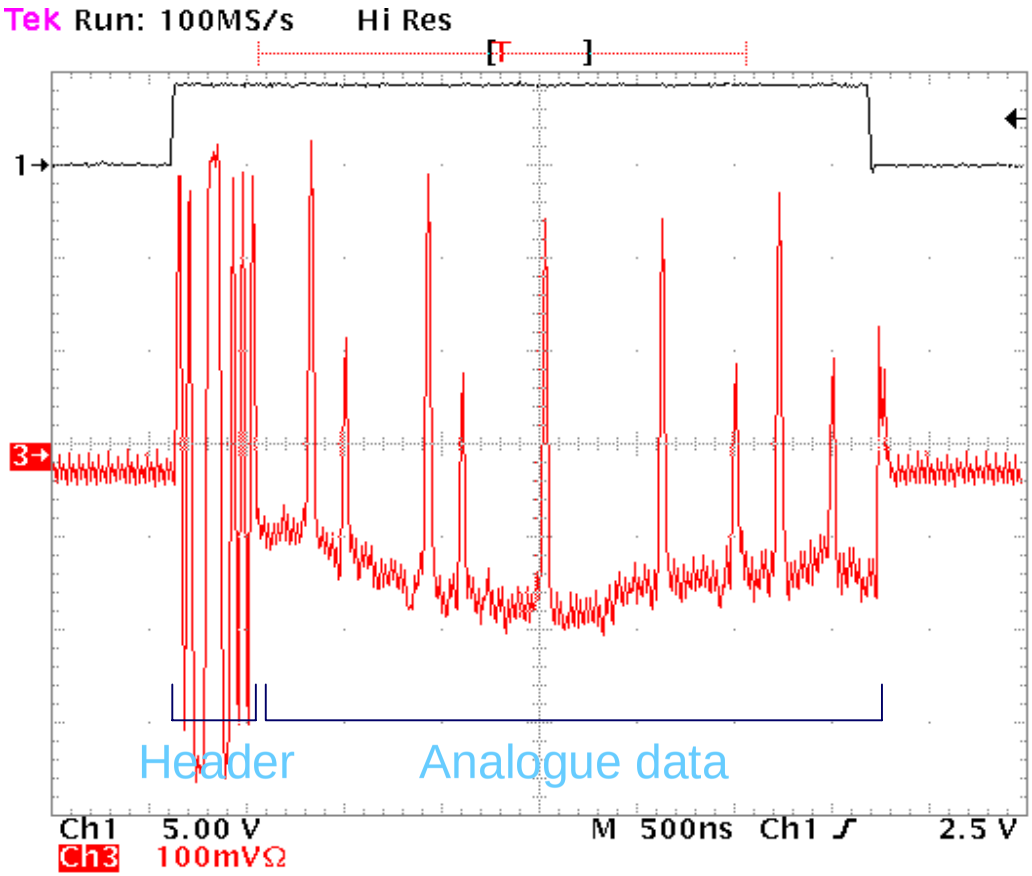
Beetle: Layout / Floor plan





Layout of the Beetle 1.2 chip and its corresponding floor plan.

Analogue readout



readout on 1 port: 16 bit header, 128 bit data

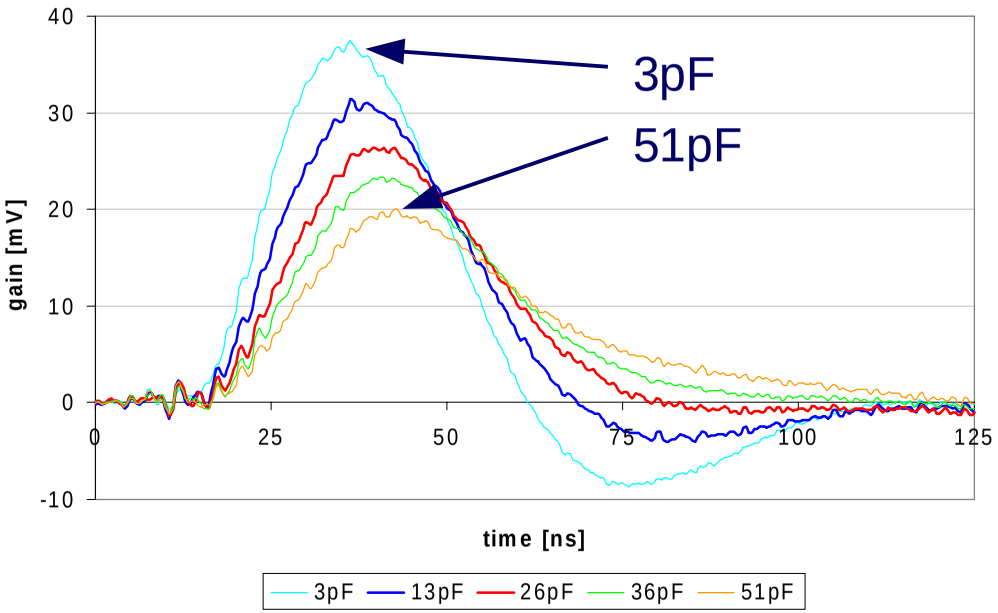
- small, but constant baseline dip
- header levels: +/- 42.150 e^- (118 e^-/mV)
- correct encoded header
  - *1 Start-bit*
  - *1 Parity-bit of Pipeline Column Number*
  - *1 EDC status-bit*
  - *3 different parity-bits of registers*
  - *2 LSB-bits of the SEU-counter*
  - *8 Pipeline Column Number (PCN) bits*

Front end: Pulseshape (1)

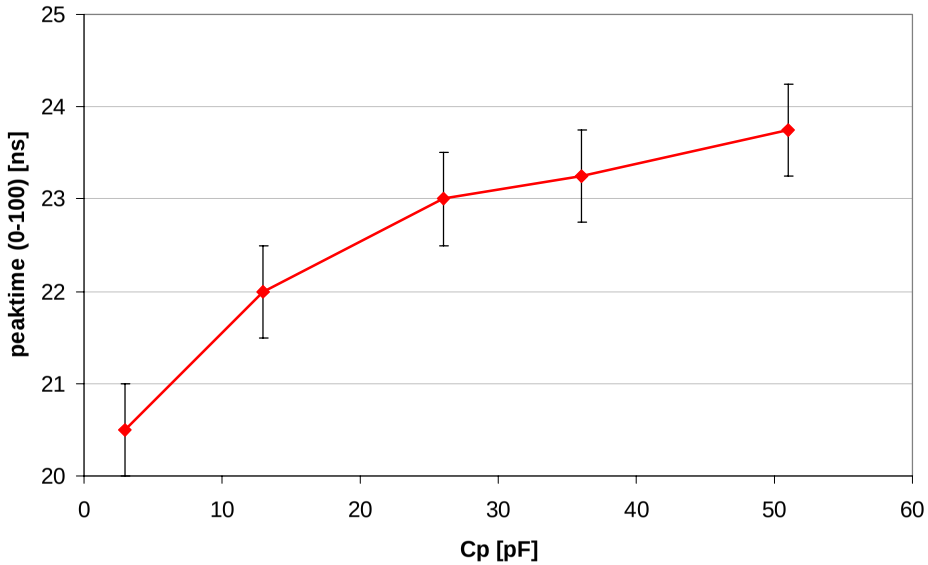
Front end behaviour of the Beetle 1.2

(measured with different Cp)

Ipre=600µA, Isha=80µA, Ibuf=200µA, Vfp=0V, Vfs=0V



peaktime (0-100)



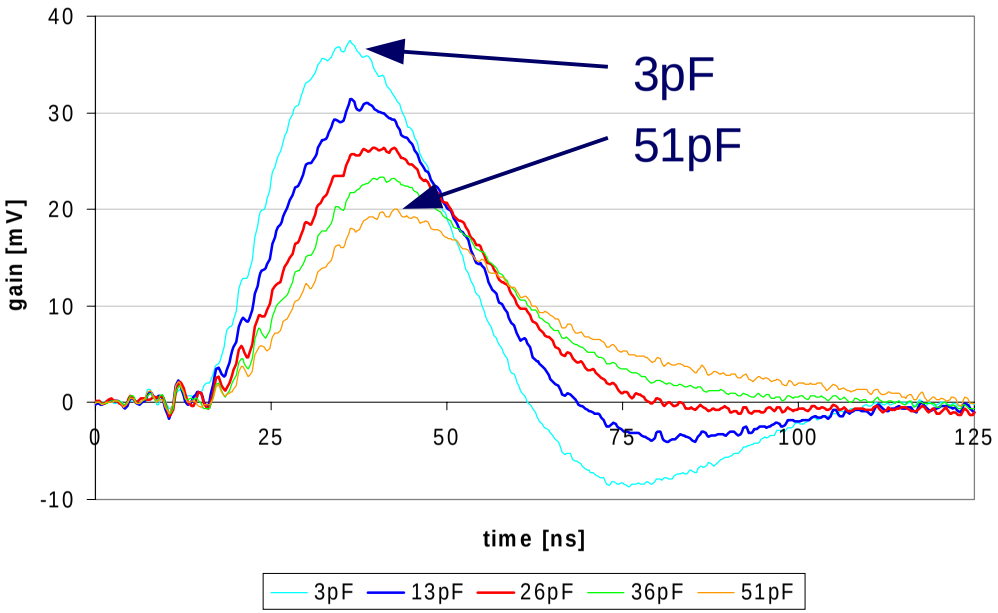
- peaktime ≤ 25 ns for $C_p \leq 51pF$

Front end: Pulseshape (2)

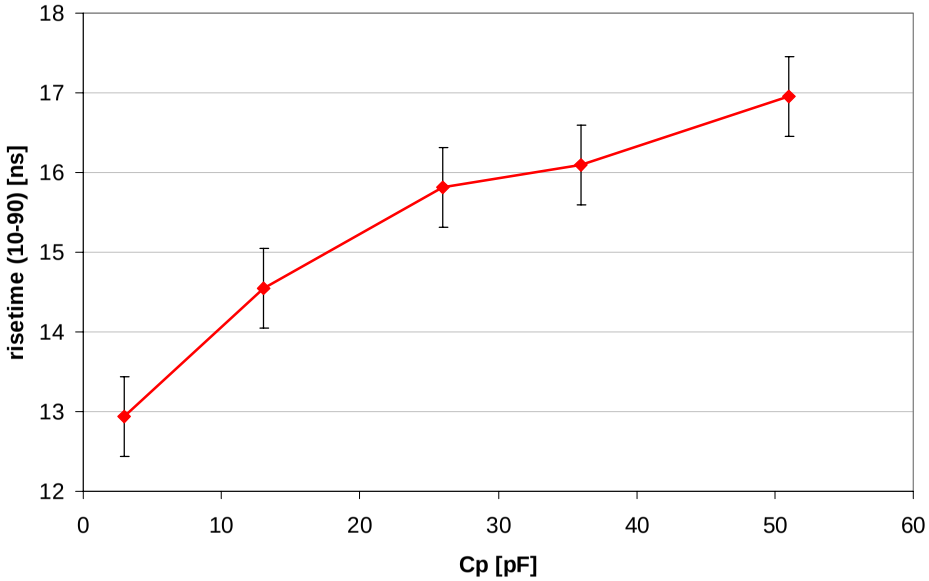
Front end behaviour of the Beetle 1.2

(measured with different Cp)

Ipre=600µA, Isha=80µA, Ibuf=200µA, Vfp=0V, Vfs=0V



risetime (10-90)



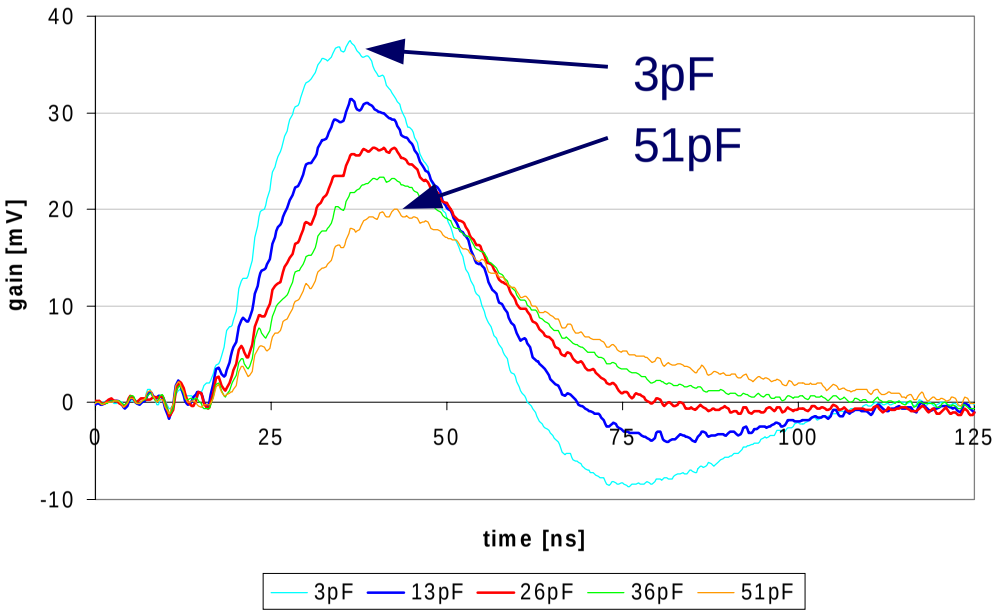
- risetime ≤ 17 ns for $C_p \leq 51pF$

Front end: Pulseshape (3)

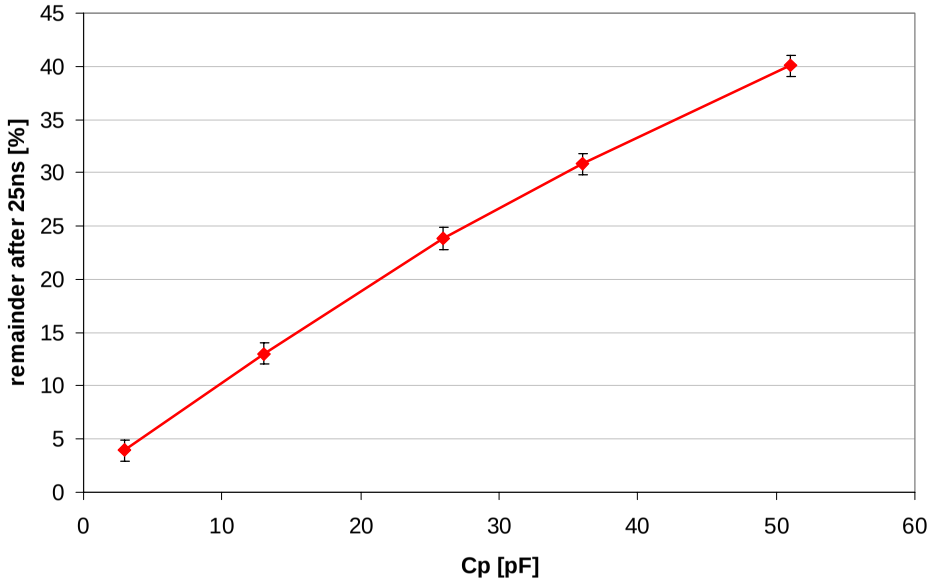
Front end behaviour of the Beetle 1.2

(measured with different Cp)

Ipre=600µA, Isha=80µA, Ibuf=200µA, Vfp=0V, Vfs=0V

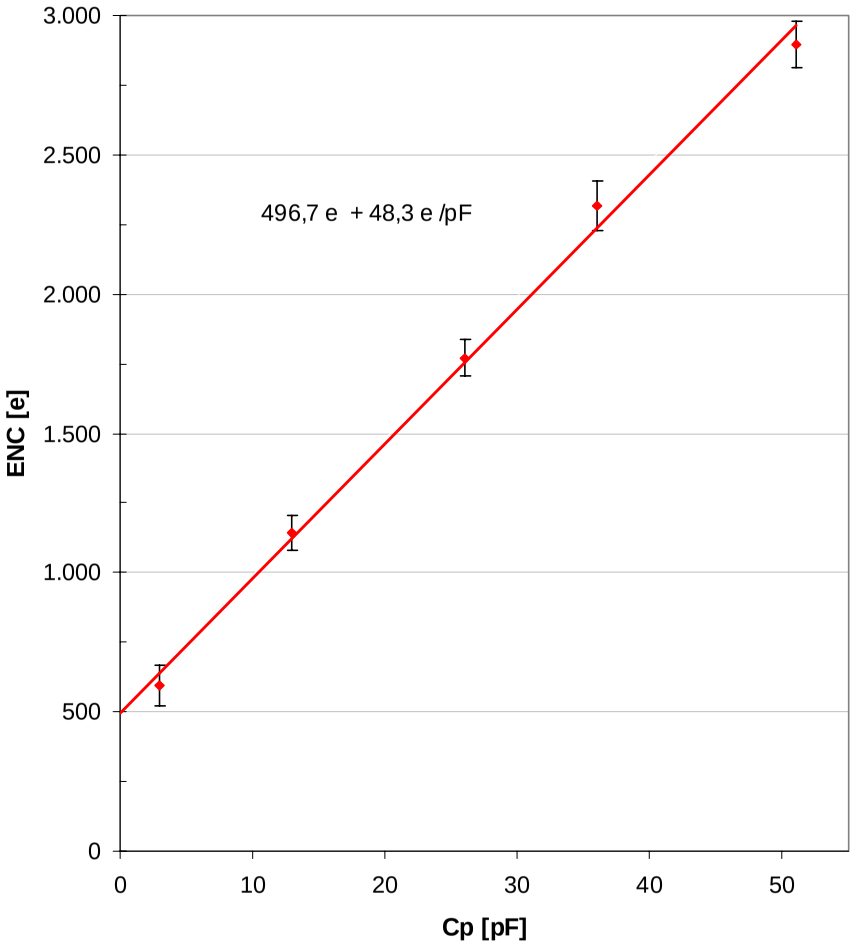


remainder after 25ns



- remainder 25 ns after peak is less than 30% for $C_p < 35pF$

Front end: ENC



p r e l i m i n a r y !

measured ENC of the new front end on a complete readout chip Beetle 1.2:

Heidelberg: 497 e^- + 48.3 e^-/pF

measured ENC of the new front end on a test chip BeetleFE 1.1:

NIKHEF:	429 e^- + 47.0 e^-/pF
Zurich:	436 e^- + 47.7 e^-/pF
Heidelberg:	483 e^- + 45.7 e^-/pF

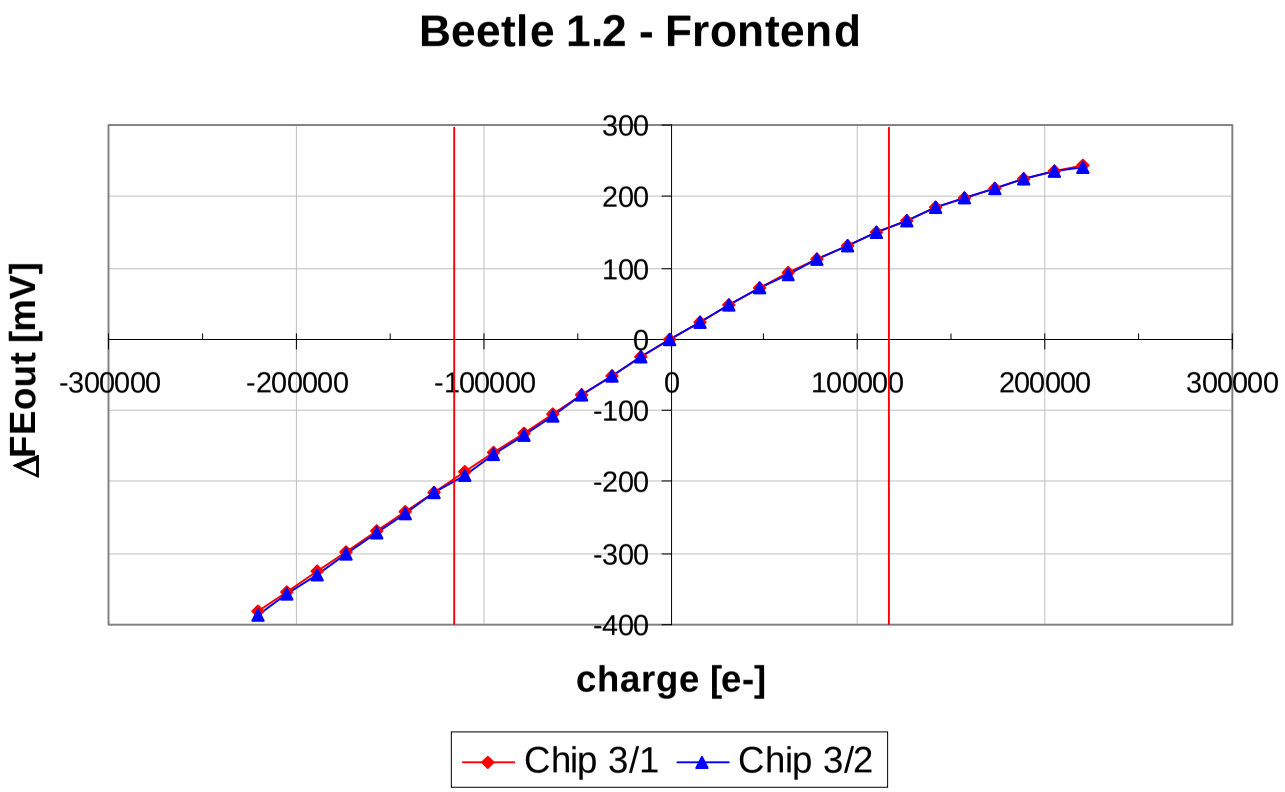
Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Front end: Dynamic range

Dynamic range for both polarities:

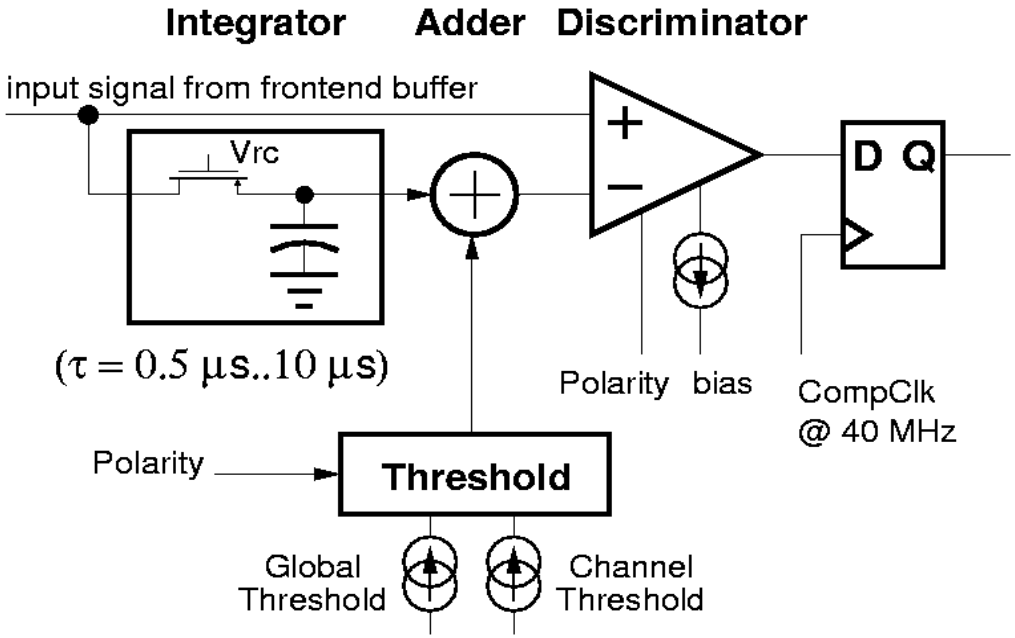
+/- 110.000 e^-: < 2% for negative pulses

< 5% for positive pulses



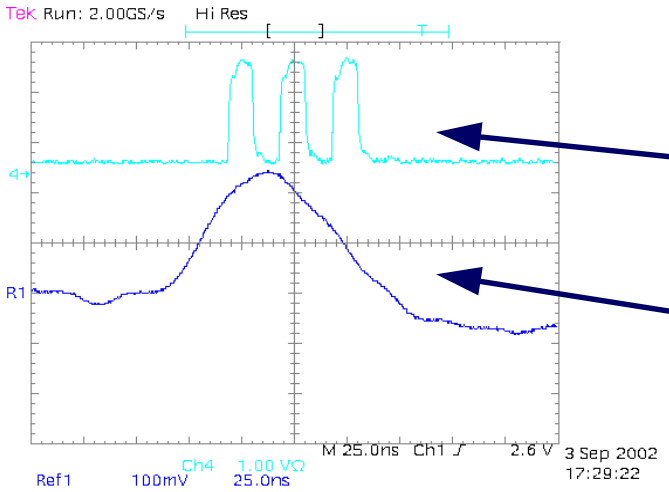
Beetle 1.2: Comparator (1)

- adjustable threshold for each channel
  - global threshold
  - channel threshold
- Integrator extracts DC-level of shaped front-end pulse and adds it to threshold
  - adjustable time-constant
- mask register for each channel
- multiple operation modes
- digital part is now SEU hard (triple redundant logic)



Beetle 1.2: Comparator (2)

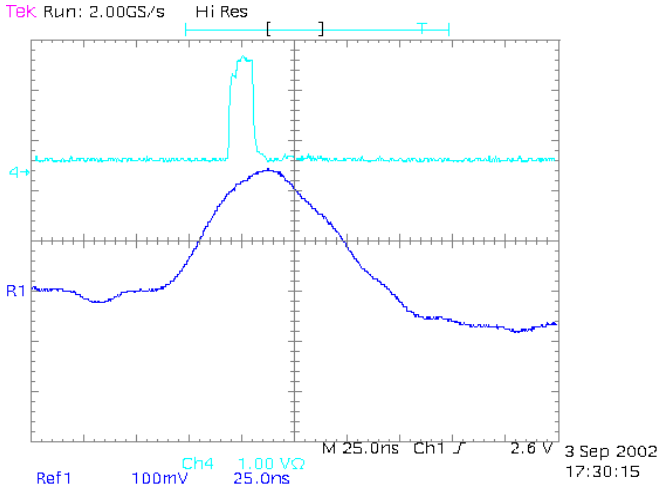
track mode
"on" as long as signal is over threshold



fast LVDS output signal

shaped front-end pulse

pulse mode
"on" only for one BX
one BX dead time



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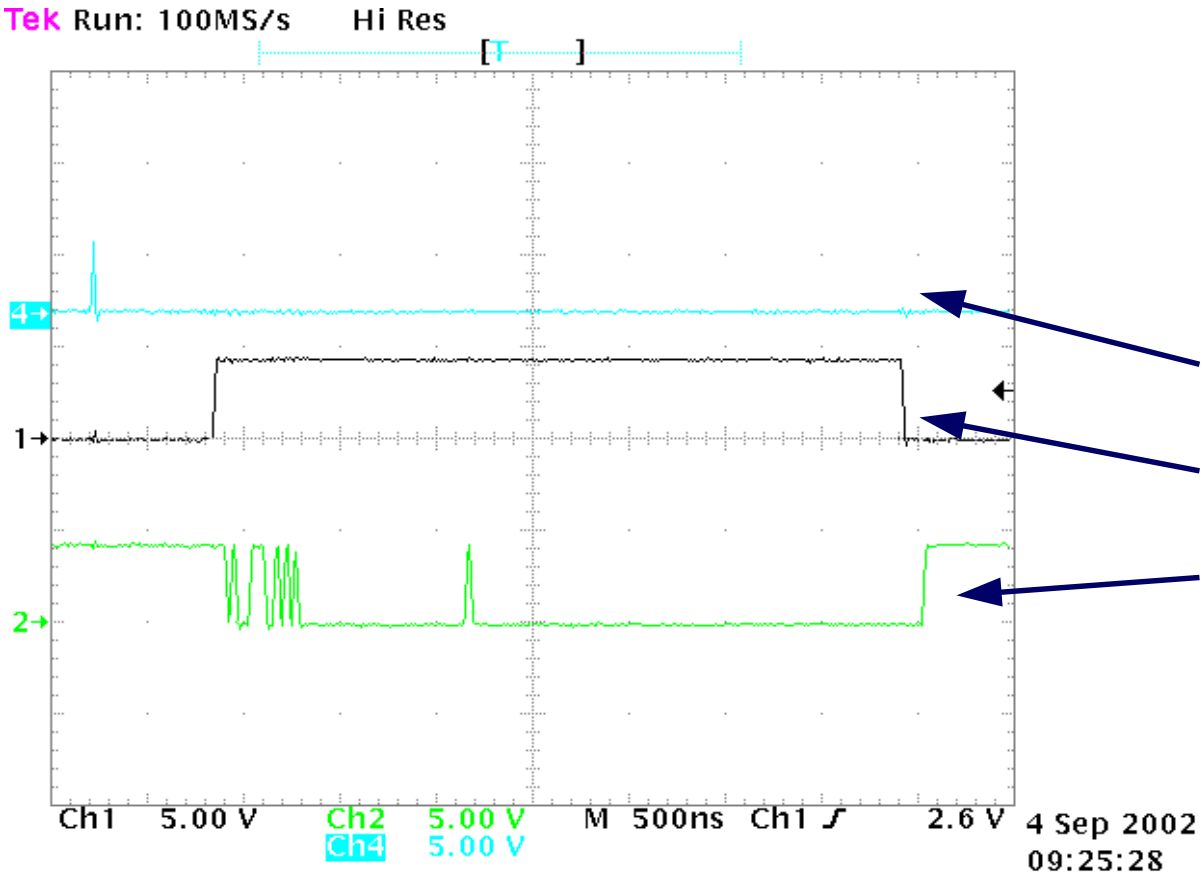
Binary readout



- **new output buffer for pipeline-mode**
  - **no signal spill-over to the next bunch crossing**

Fast comparator output (LVDS signal)

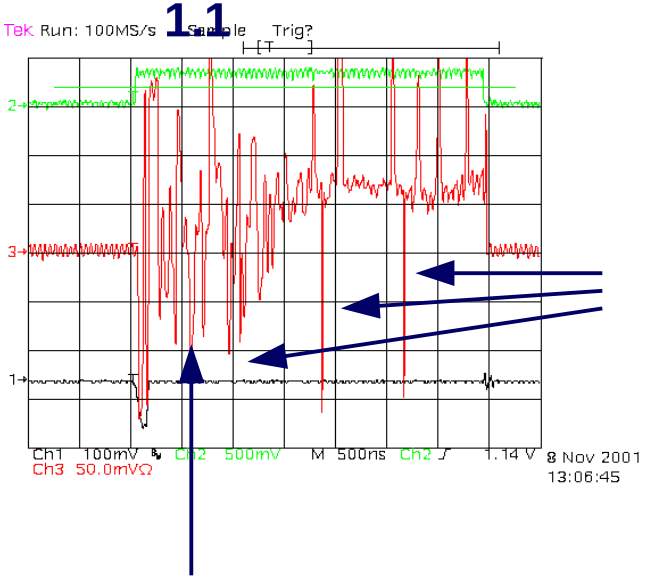
DataVaild (LVDS signal)

Comparator in pipeline-mode
Analogue output pads switched to LVDS output pads

Low trigger rate

Readout at trigger rates of 1 Hz and below

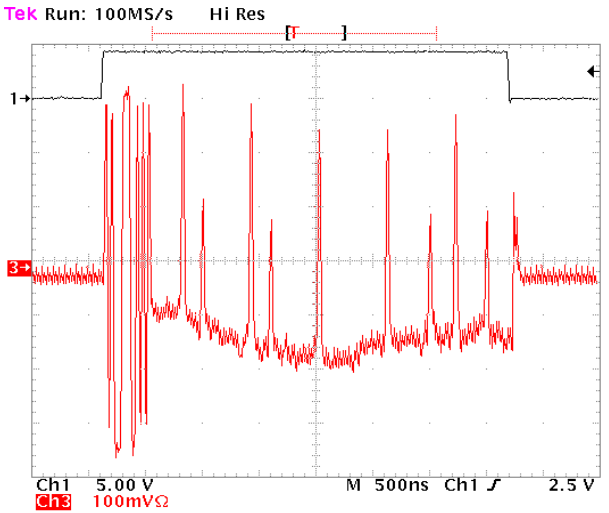
Beetle 1.1

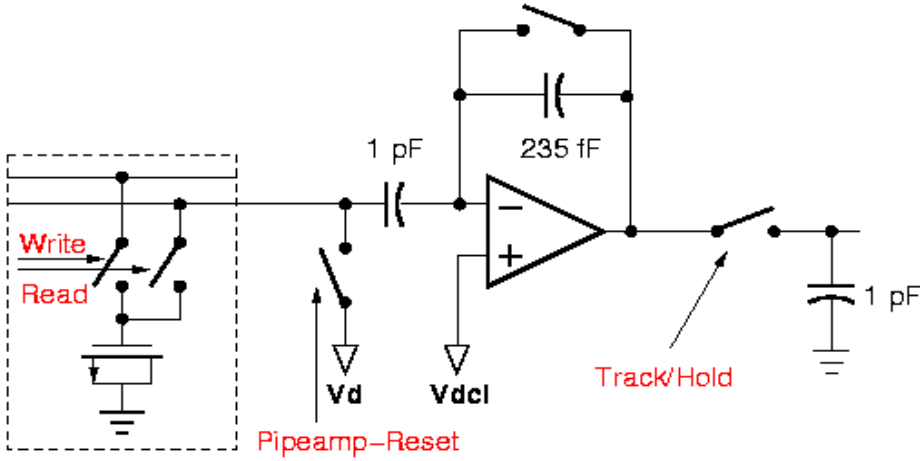


Occurs only in 128 channels on 1 port output mode

Floating wire between Pipeamp and MUX
⇒ wrong DC operation point at the beginning of a readout

Beetle 1.2





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Output Driver / Modes

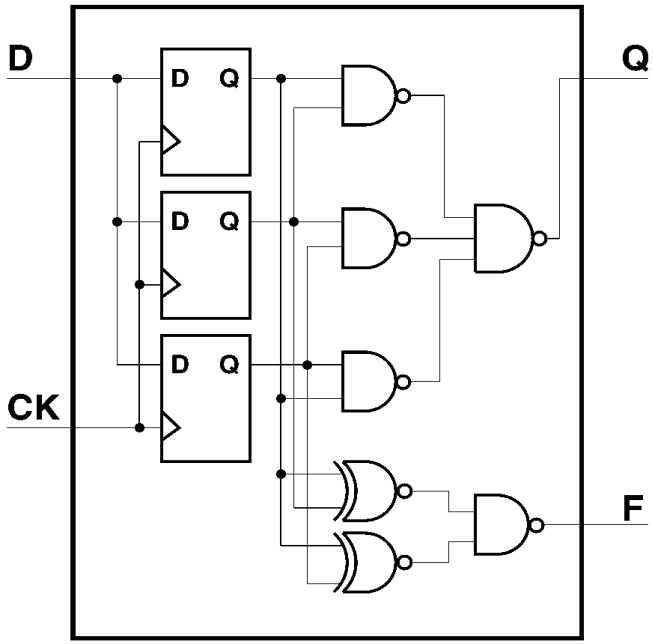
- Analogue Output Driver
  - bidirectional current driver
  - designed to drive analogue signals more than 10 m
- Binary Output Driver
  - implemented as LVDS transceiver
  - used for the digital pipelined comparator signals

same output pads for both output drivers

- Modes of output operation
  - on 4 ports @ 40 MHz in parallel: readout in 900 ns
  - on 2 ports @ 80 MHz in parallel: readout in 900 ns
  - on 1 port @ 40 MHz: readout in 3.4 µs (for test purposes)

Beetle 1.2: Biasing

- DAC resolution reduced from 10 bit to 8 bit
- Doubled the max. output current of all Current DACs from 1 mA to 2 mA
- Self triggered, triple redundant flip-flops in all bias registers => Hardened against SEU



triple redundant flip-flop with flip indication

Fast control / Slow control

- Slow control (I^2C-Interface and Register Control)
  - Hardened against SEU *(state machines use triple redundant flip-flops with majority encoding)*
  - Hard wired 7-bit Chip Id.
  - 20 write- and readable 8-bit registers
  - 3 write- and readable mask-registers (in total 641 bits)
  - 1 SEU counter (8-bit). *(counts all detected and corrected SEU flips).*
- Fast control (Pipeline and Readout Control)
  - SEU hard
  - New reset schema *(only one external reset; internal power-up resets all bias and state registers)*
  - New control schema of the Pipeamp / MUX to prevent the sticky charge problem at low trigger rates.
  - Trigger is latched internally (“Trigger phasing”)
  - Daisy-Chain concept is now implemented
  - New 8-bit analogue readout header *(Start-bit, Parity-bit, EDC status-bit, 3 different parity-bits of registers, 2 LSB-bits of the SEU-counter)*

Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Total Ionizing Dose irradiation

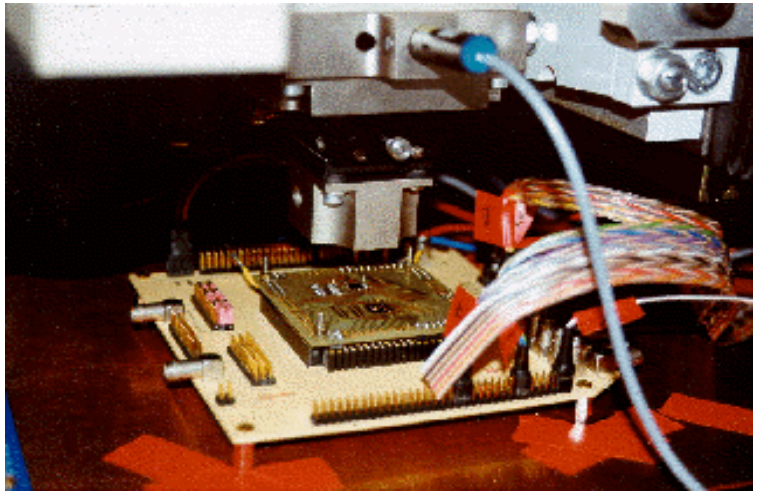
Done at the X-ray facility of CERN's Microelectronic Group

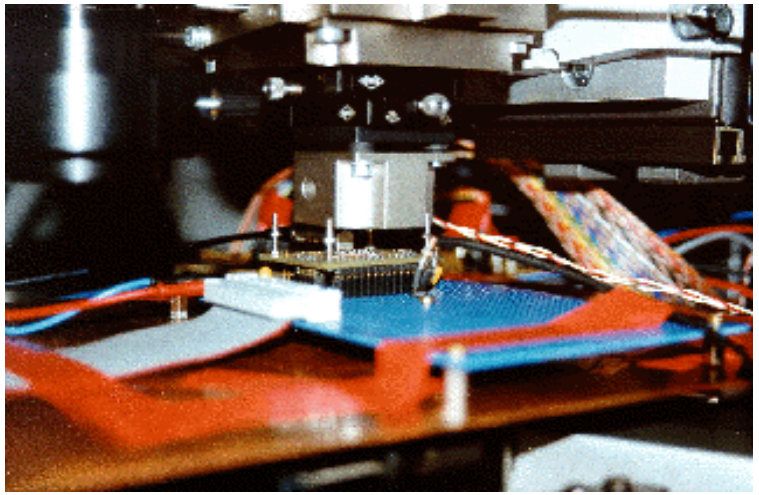
Irradiated Chips:

- **4 Beetle 1.1 chips**
  - 2 chips being kept at room temperature
  - 2 chips being annealed at 100 °C
- **2 BeetleFE 1.1 chips**
  containing FE prototypes with a NMOS input transistor
- **2 BeetleFE 1.2 chips**
  containing FE prototypes with a PMOS input transistor

Accumulated Dose:

- **Beetle 1.1:** 10 Mrad, 10 Mrad, 30 Mrad, 45 Mrad
- **BeetleFE 1.1:** 10 Mrad
- **BeetleFE 1.2:** 10 Mrad



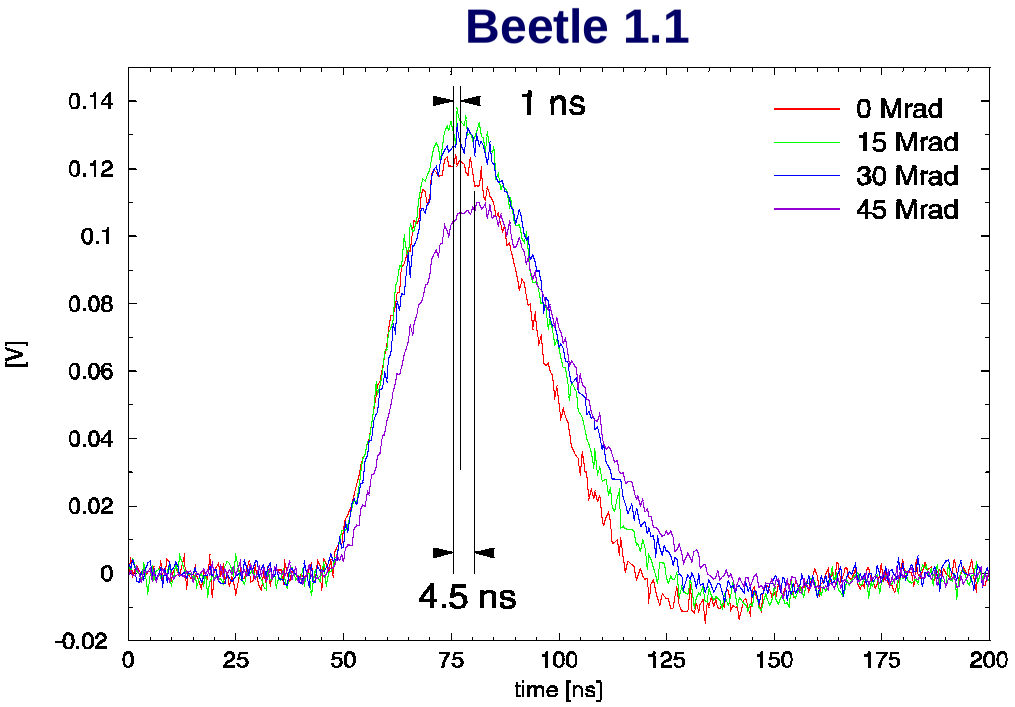


TID: Results of Beetle 1.1

Beetle 1.1 showed full functionality beyond 45 Mrad

- full trigger and readout functionality
- full slow control functionality
- performance degradations are small
  - peaktime: up to 30 Mrad: ≤ 1 ns
    up to 45 Mrad: ≤ 4,5 ns
  - gain: up to 45 Mrad: ≤ 10%

no tuning of bias settings



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Summary

Internal Testpulse	as expected
New Front-end	as expected
Comparator	functionality tested
Pipeamp / MUX	performance problems with consecutive readout
Analogue / Digital Output Driver	as expected
I^2C / Slow Control	as expected
Fast Control	OK for LHCb
DACs / Biasing	as expected
New Pads (I^2C, CMOS, monitoring-pads)	as expected

Sven Löchner
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