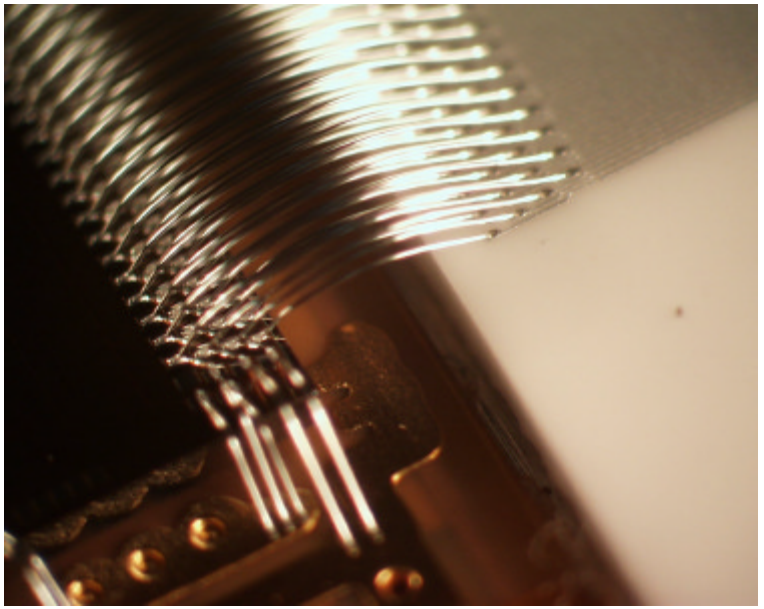
Lab measurements with the Beetle 1.3 - Update -

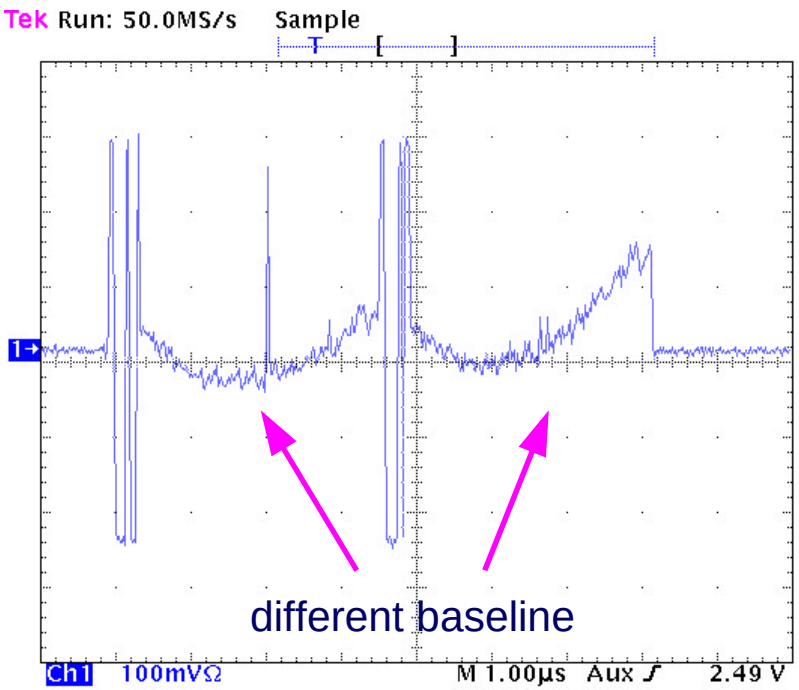
Sven Löchner

(Max-Planck-Institute for Nuclear Physics, Heidelberg)

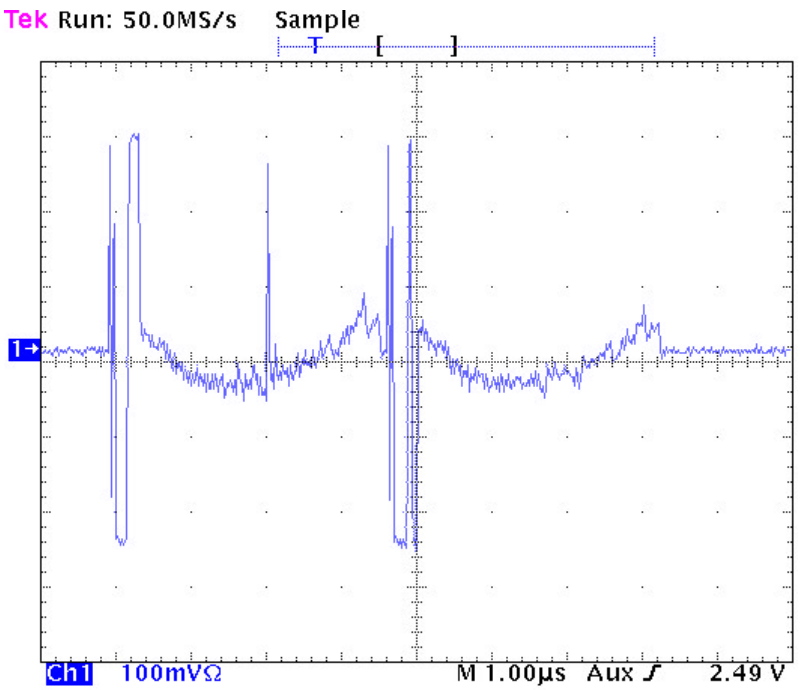


Beetle 1.3
128 staggered input bondings

Readout



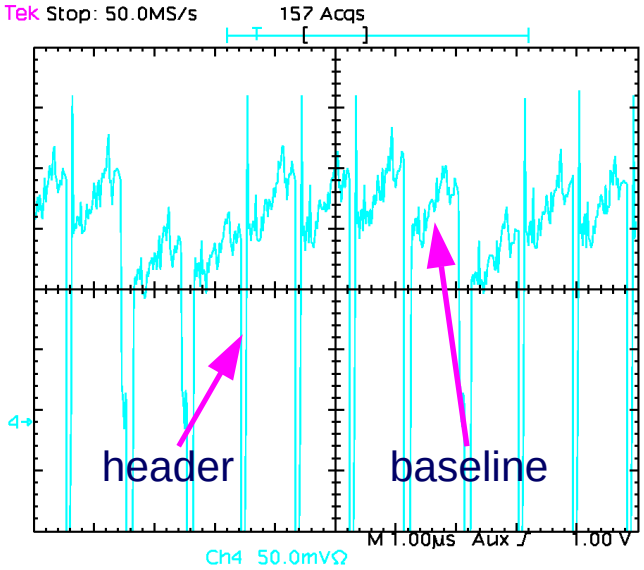
consecutive readout



non-consecutive readout

Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

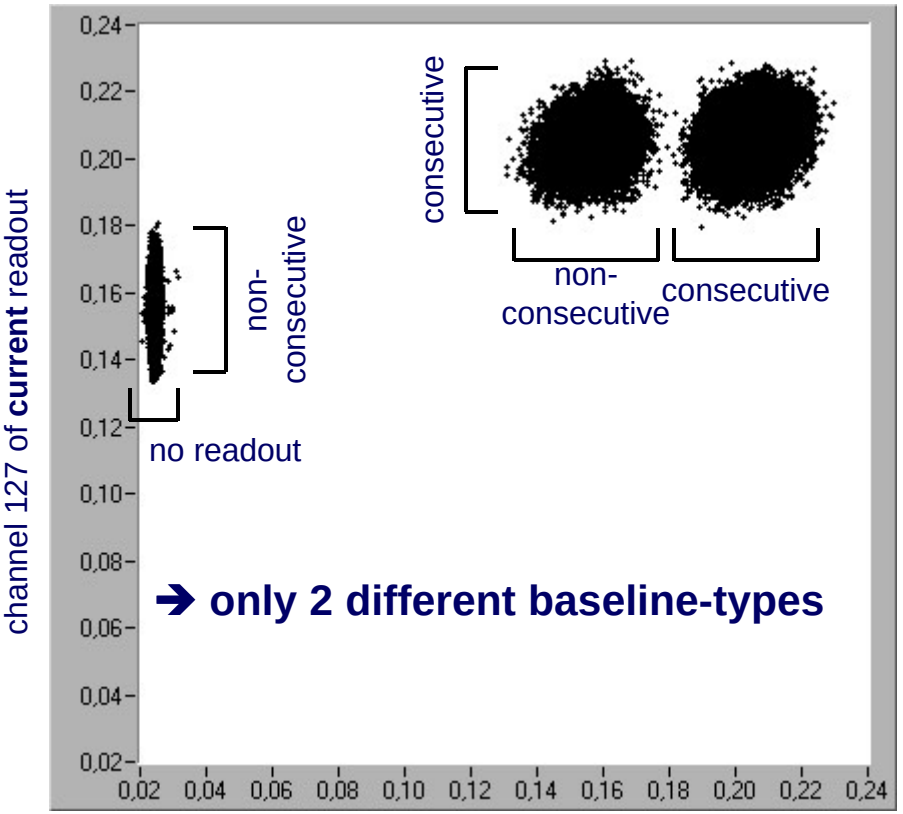
Readout (Baseline) I



AnalogOut<3> - channel 96 to 127

- **32 channels on 4 port (LHCb-mode)**
- **non-consecutive & consecutive RO**

previous readout vs. current readout

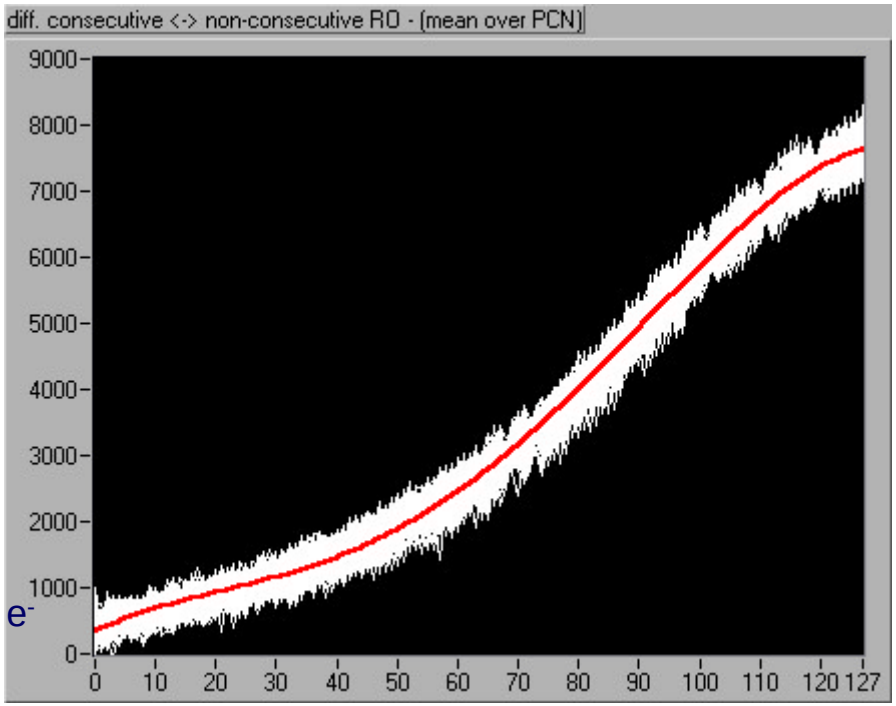


Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Readout (Baseline) II

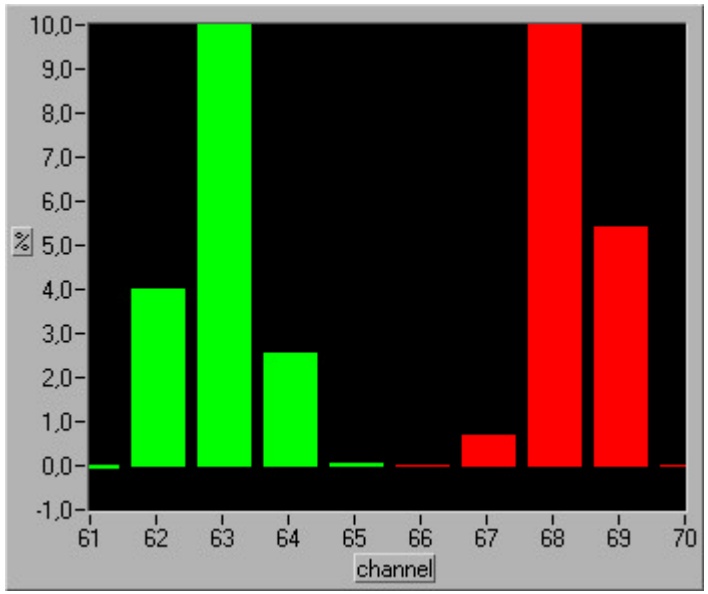
- **32 channels on 4 port (LHCb-mode)**
- **consecutive minus non-consecutive RO**

delta consecutive / non-consecutive RO



Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Channel Crosstalk (1)



Testpulse (63. & 68) is standardised to 100%

Channel crosstalk

- **measured a even/odd dependency**
- **this effect is also present in 1.2**

Clarification of crosstalk:

typical Testpulse for a odd channel (e.g. 63):
crosstalk into predecessor channel is larger than into successor channel

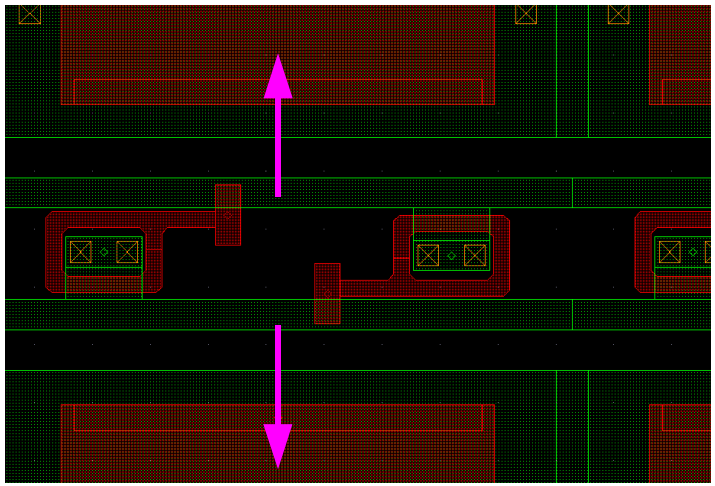
typical Testpulse for a even channel (e.g. 68):
crosstalk into successor channel is larger than into predecessor channel

Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Channel Crosstalk (2)

Channel crosstalk is a superposition of at least two different crosstalks:

- **general “remainder” into next readout channel (order of 2% to 2.5%)**
  - **➔ reason not understood (maybe MUX?)**
- **odd channel: crosstalk into predecessor ch.**
  even channel: crosstalk into successor ch.
  (order of 2.5 %)
  - **➔ readout line from Pipeline into Pipeamp**
    capacitance between adjacent lines ~ 60fF
    - **verified in simulation**
    - **easy to fix (stretch lines)**



Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Readout header: parity bit

1 port mode

AO[0]	I0	I1	I2	I3	I4	I5	I6	I7	P7	P6	P5	P4	P3	P2	P1	P0

4 port mode

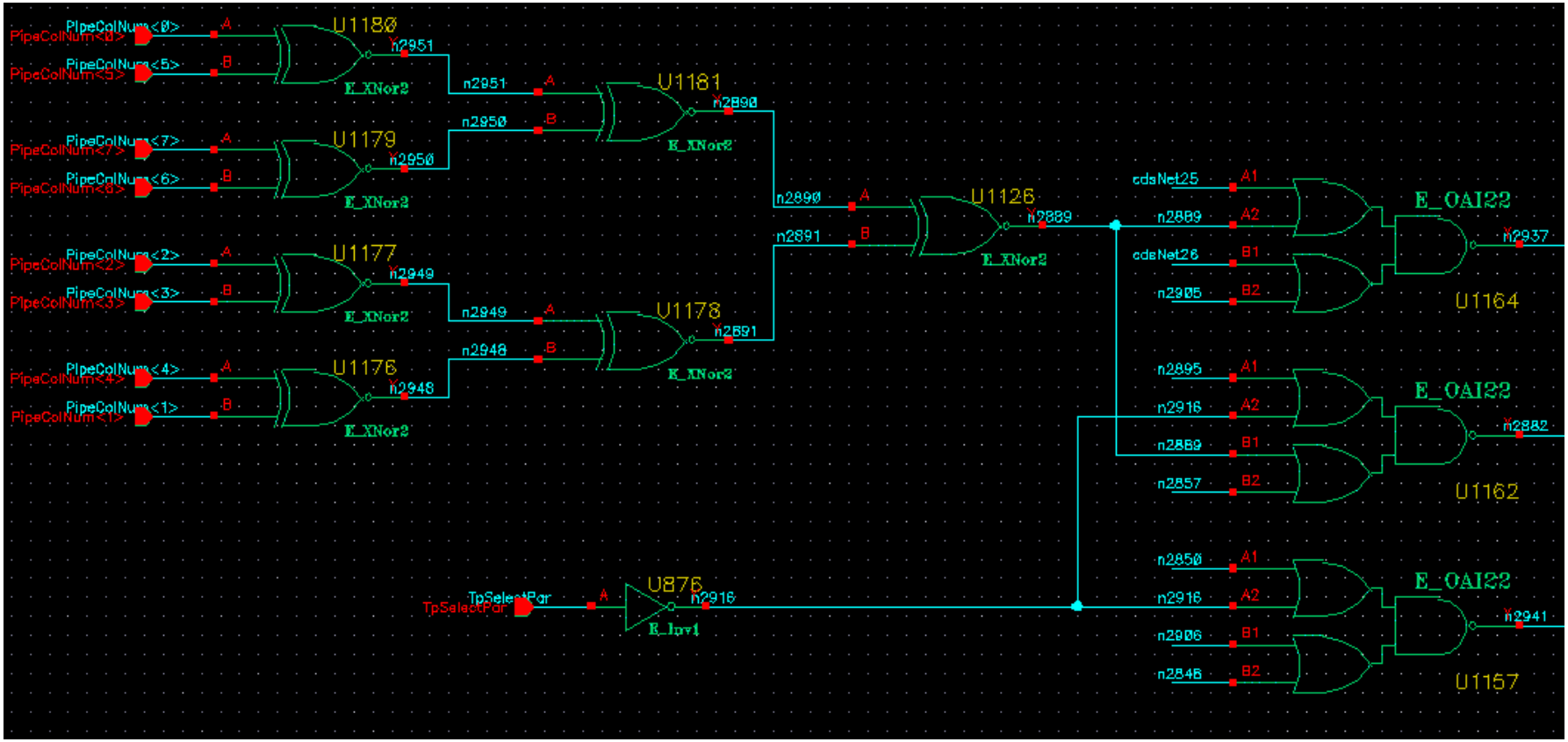
AO[0]	I0	I4	P1	P0
AO[1]	I1	I5	P3	P2
AO[2]	I2	I6	P5	P4
AO[3]	I3	I7	P7	P6

I0	leading bit (always 0)
I1	parity of PCN (even)
I2	Active EDC
I3	parity of reg. CompChTh
I4	parity of reg. CompMask
I5	parity of reg. TpSelect
I6	SEU counter <1>
I7	SEU counter <0>

- **Parity bit (I1) is wrong encoded in 4 port mode and Rclk divider = 0 (LHCb mode)**
- **all other modes or Rclk divider settings**
  ➔ Parity bit is OK
- **problem is understood in verilog**
  - **not so easy to fix**
  - **simple workaround: swap position I1 with I5 could be tested on a 1.3 with a FIB patch**

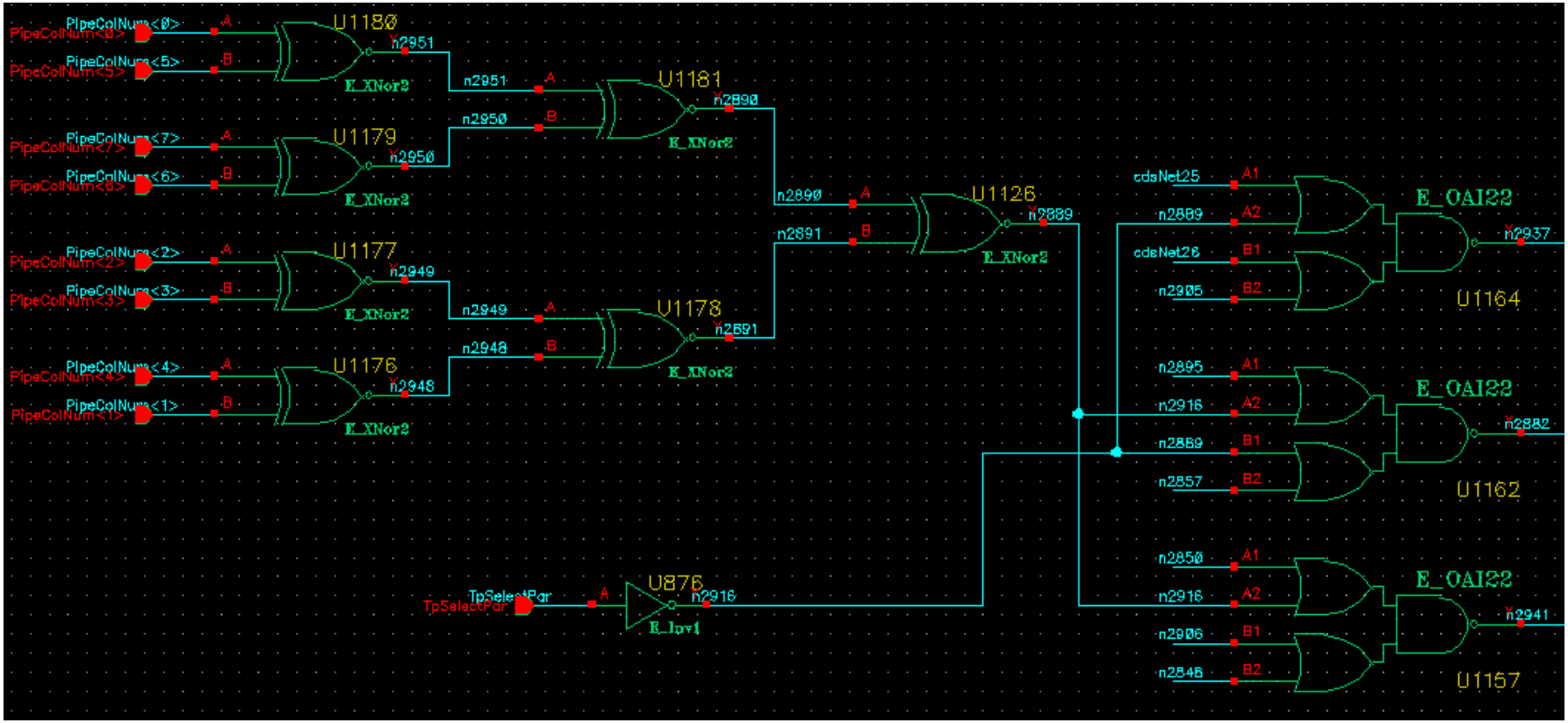
Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Parity bit - workaround (1)



schematic of parity-bit generation (part of MuxScheduler)

Parity bit - workaround (2)

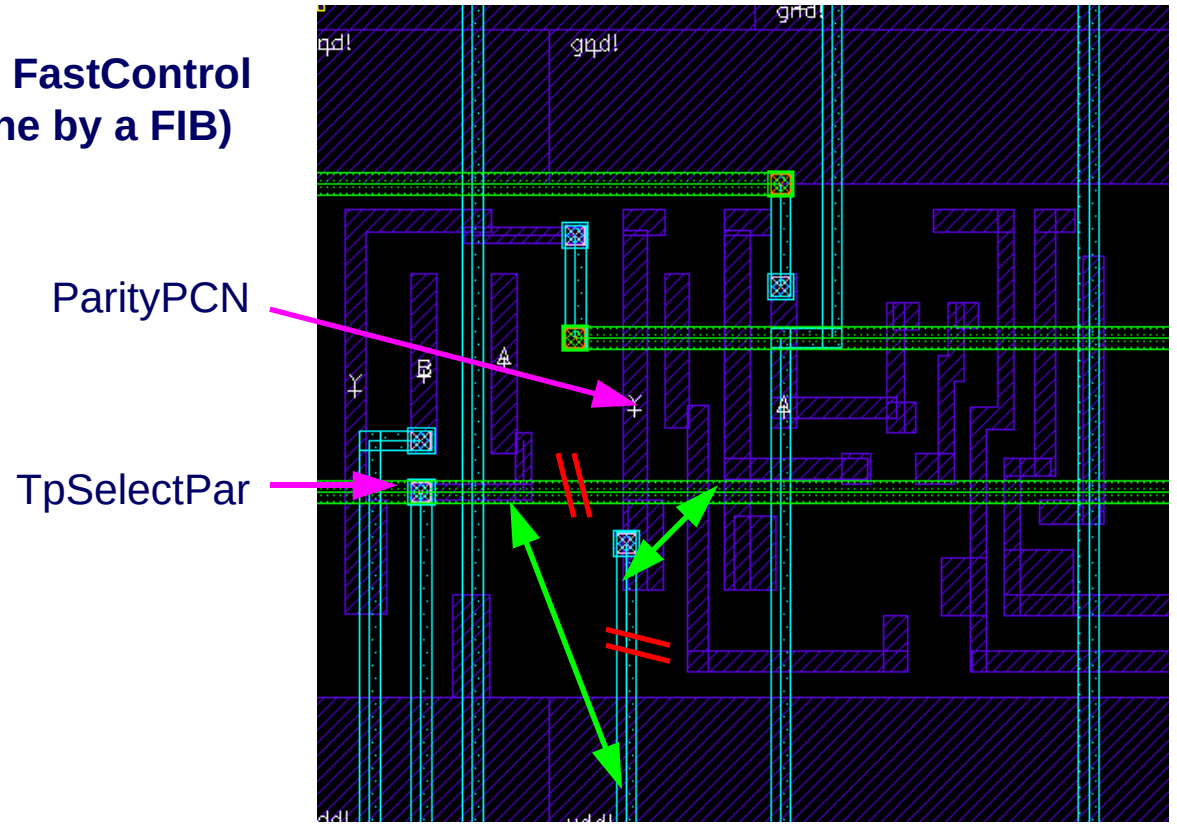


new schematic of parity-bit patch

Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg

Parity bit - workaround (3)

- **Layout modification in FastControl of Beetle (could be done by a FIB)**
  - **2 cuts**
  - **2 connections**



Output device of ParityPCN generation - E_XNor2 (U1126)

Sven Löchner
ASIC-Laboratory, Max-Planck-Institute for Nuclear Physics Heidelberg