FrontEnd Electronics Development for LHCb

Status Report and Future Plans

Reminder: general strategy

Main line of development:

Beetle (IBM 0.25 um CMOS):

dedicated readout chip for the vertex detector, inner tracker, pile-up trigger, RICH

Fallback solution:

SCTA (DMILL 0.8 um BiCMOS):

existing design will be modified to match the LHCb requirements

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SCTA modifications:

existing design
- Latency: 118
- # of multi event buffers: 8
- setup time for readout: 500ns
- 128 channels read out serially

modifications for LHCb:

1.) Multiplexer splitting
4 outputs with
2 bits pipeline address as header
32 channels analog data

2.) Change of sequencer to reduce setup time
compatible with a readout rate of 1MHz

3.) Latency inreased to 160 / multi event buffer to 16

4.) I2C interface for register programming added

Part 1.) & 2.) being worked on by
Jan Buytaert and Edgar Sexauer
planned to be ready by end of 7/99

submission planned to be in 2/2000

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Beetle specifications:

- readout via 4 channels with 32 slots
  plus 2 bit header containing the pipeline address
- latency of 160 cells
- serial programming by I2C interface
- optional binary readout both immediately and pipelined
- intensive test and monitoring facilities

done so far:

- design of a frontend amplifier with 25ns shaping time
- design of bias generators and current sources
- chips expected to be back from fabrication end of 7/99

further steps:

- submission of pipeline including control logic
  by the end of 1999
- submission of a readout chip planned for 10/2000
- second iteration planned for 10/2001

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task assignement for Beetle development:

- Martin Feuerstack-Raible, Michael Schmelling:
  coordination
- Nigel Smale
  RICH specific frontend, digital control circuit
- Niels van Bakel
  development of SVD specific frontend,
  fast comparators for pile-up veto
- Edgar Sexauer
  fast readout scheme and output buffers