Status of Investigations on Beetle1.2 and Steps Towards Beetle1.3

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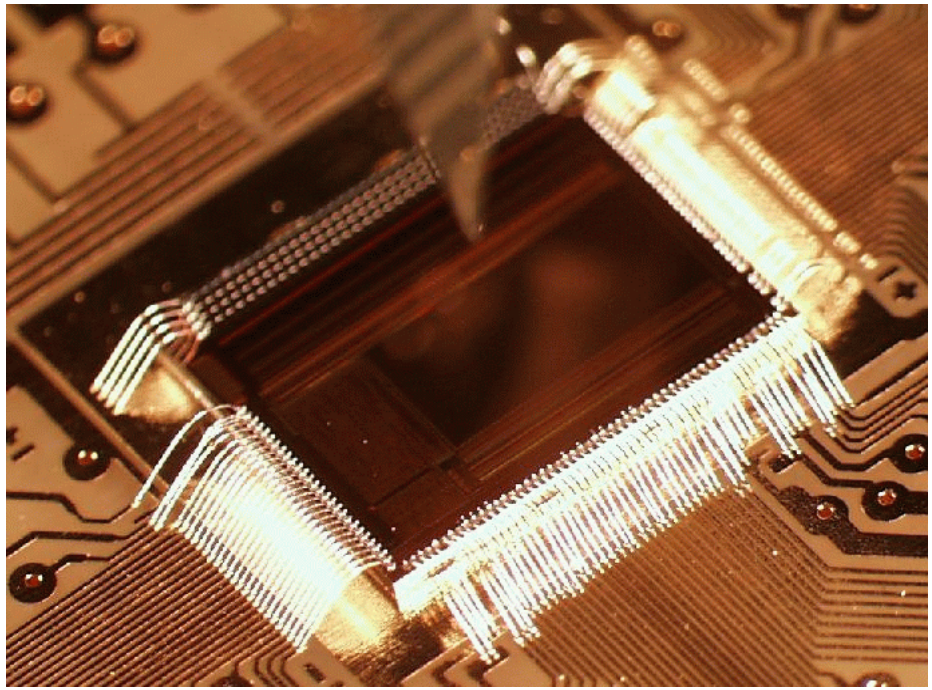
Outline

- Sticky Charge Effect
- 80 MHz Cross Talk
- Sagging Readout Baseline
- Modifications to the Comparator
- Chip size
- Further Issues



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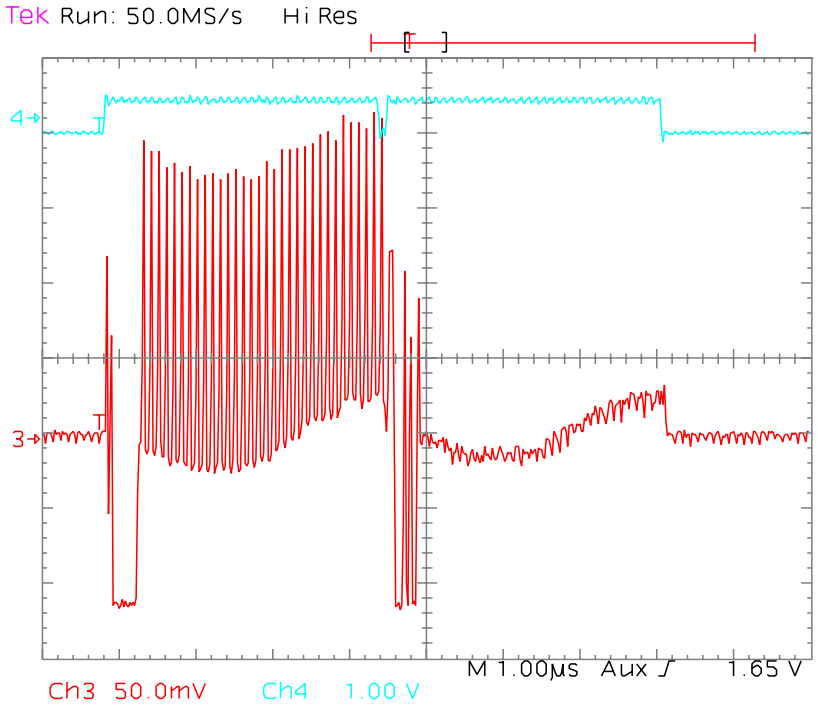
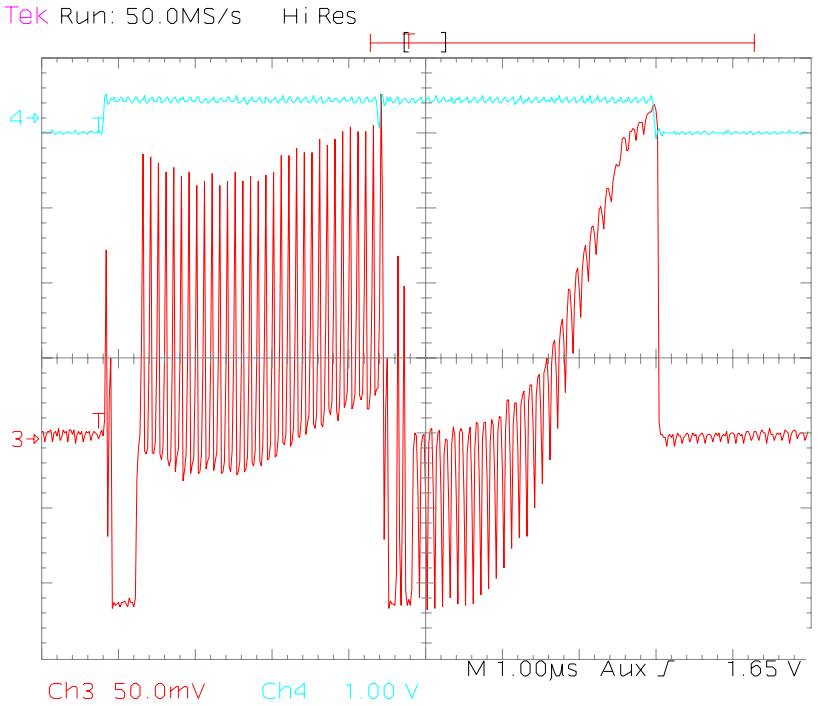
Sticky Charge Effect (1)

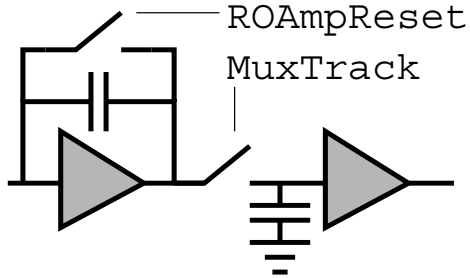
- signal carry−over from previous event into an empty event, strong baseline drift
- only present for consecutive readouts, i.e. during a readout operation a further trigger arives

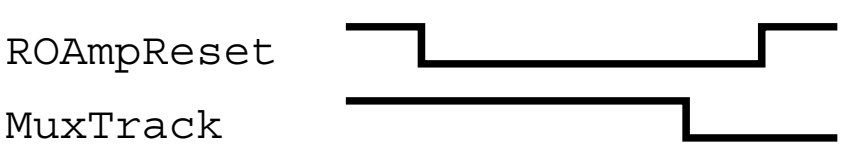
non−consecutive readout

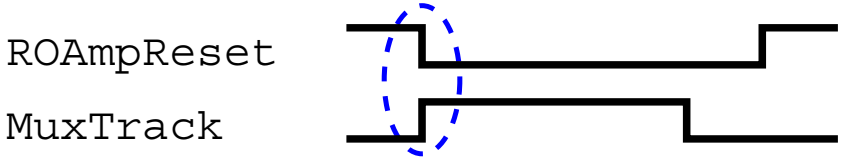


consecutive readout









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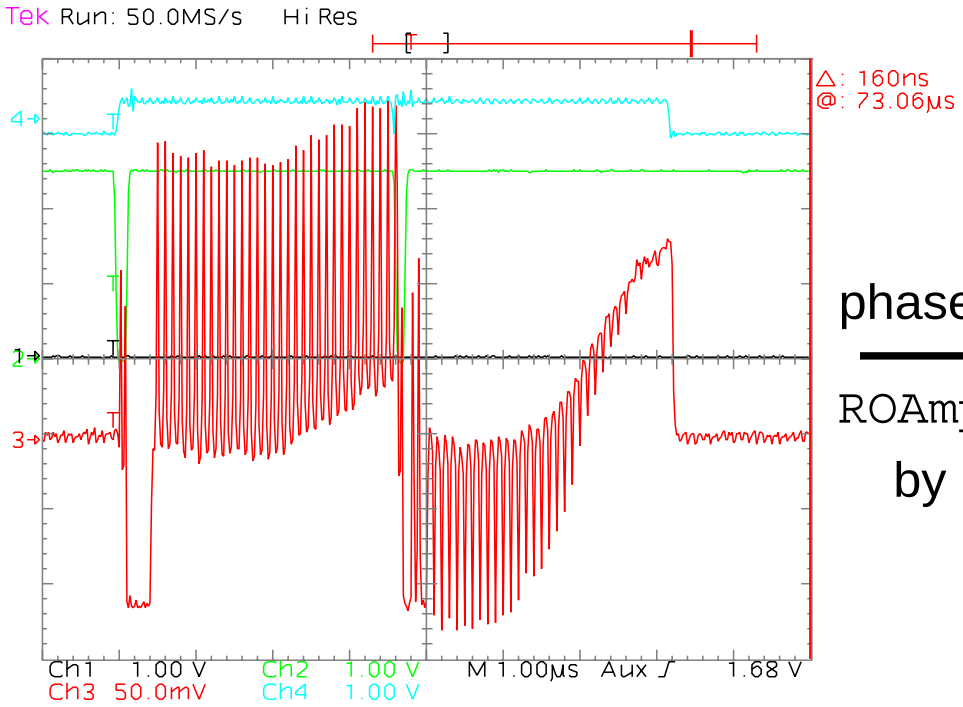
Sticky Charge Effect (2): Laser Patch

- polyamide/nitride/oxide window has been opened using UV−laser
- probe−needle has been positioned onto the reset line of pipeamp (ROAmpReset)
- external signal has been superimposed to the internal signal pulse
- phase of the external reset pulse relative to the clock has been varied

consecutive readout

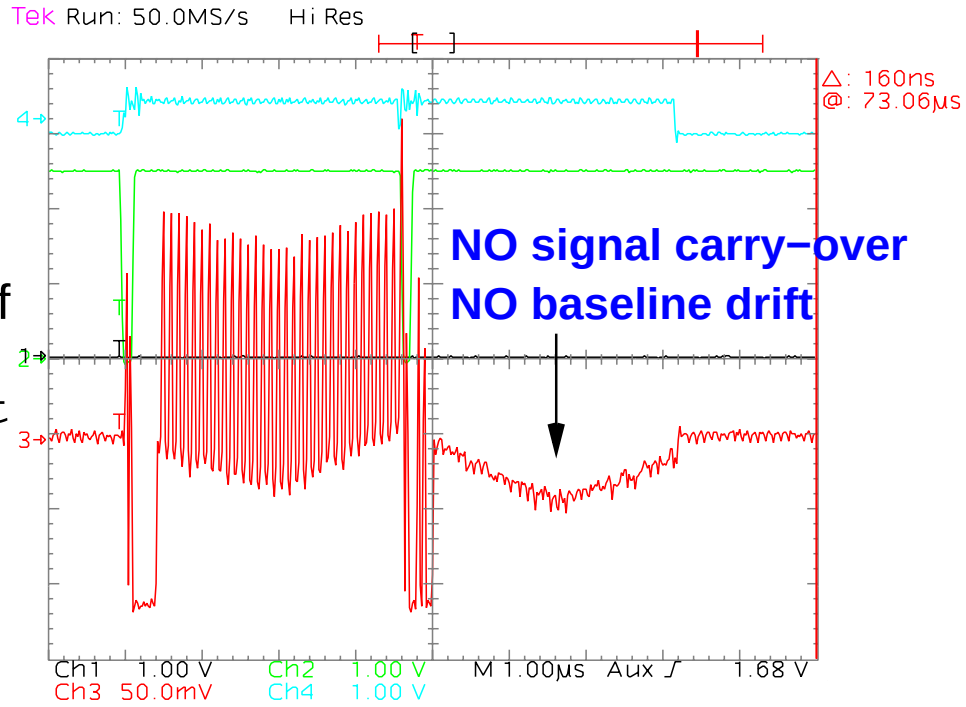


phase shift of

ROAmpReset

by 10 ns

consecutive readout



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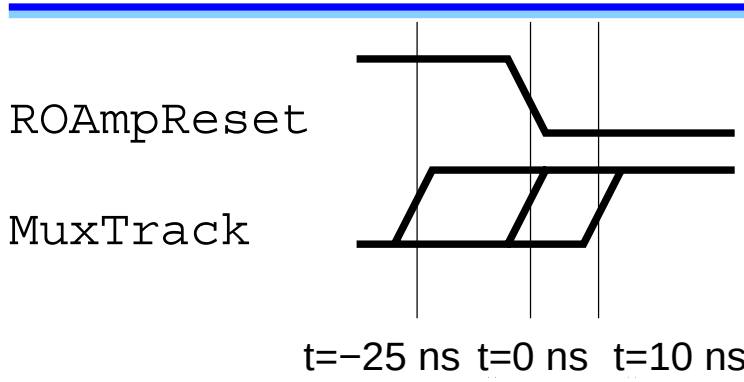
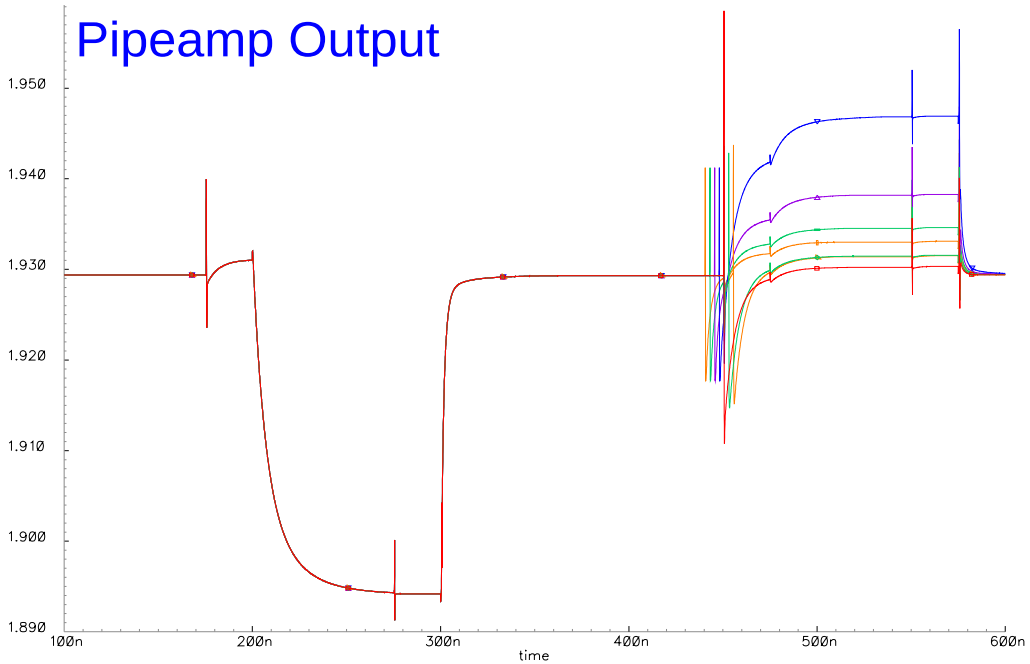
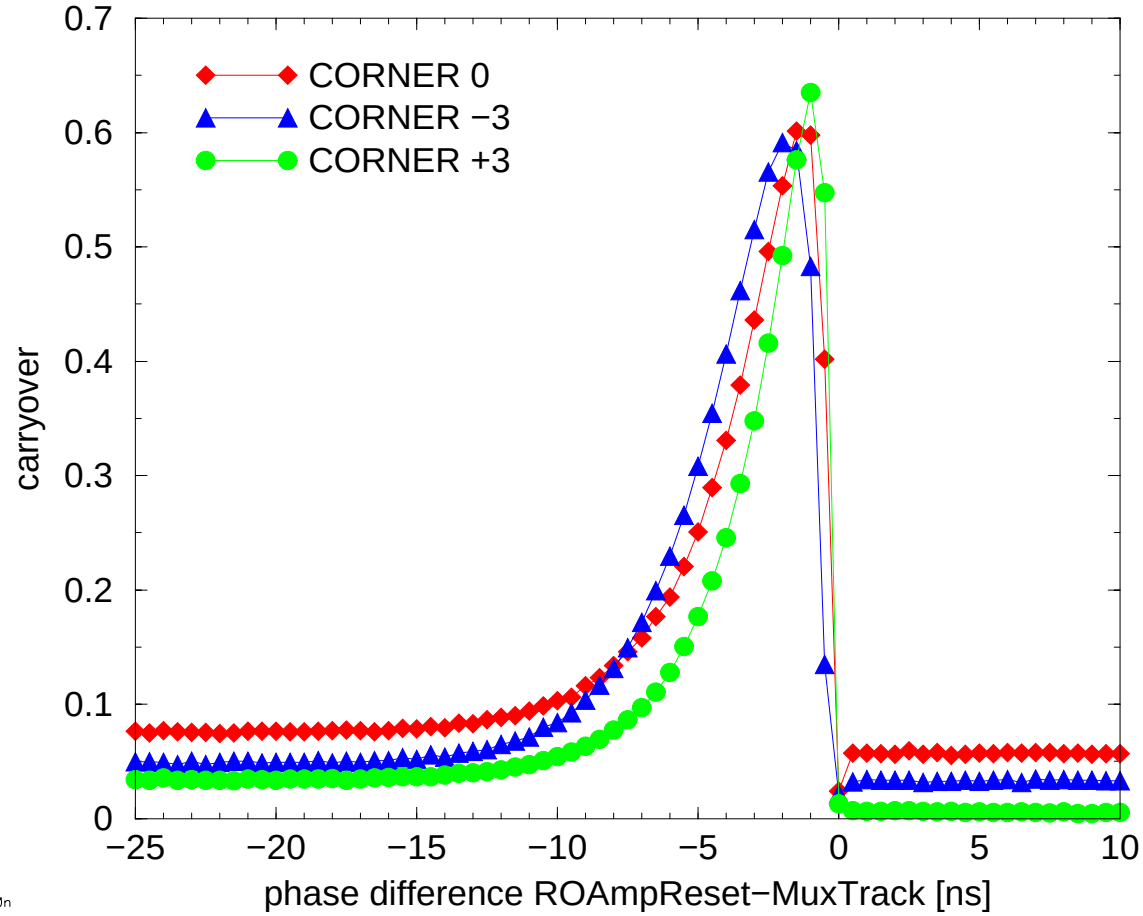
Sticky Charge Effect (3): Simulations







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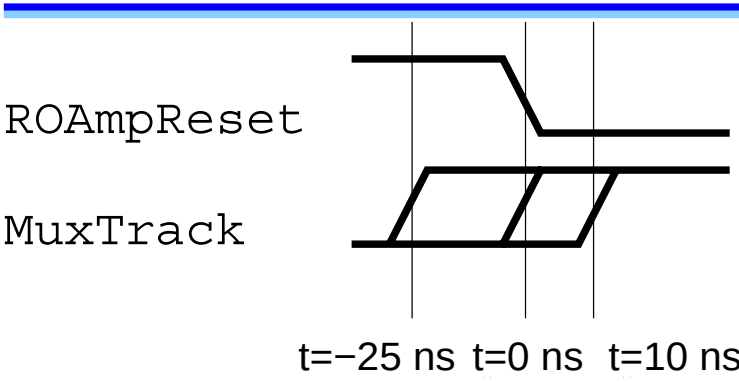

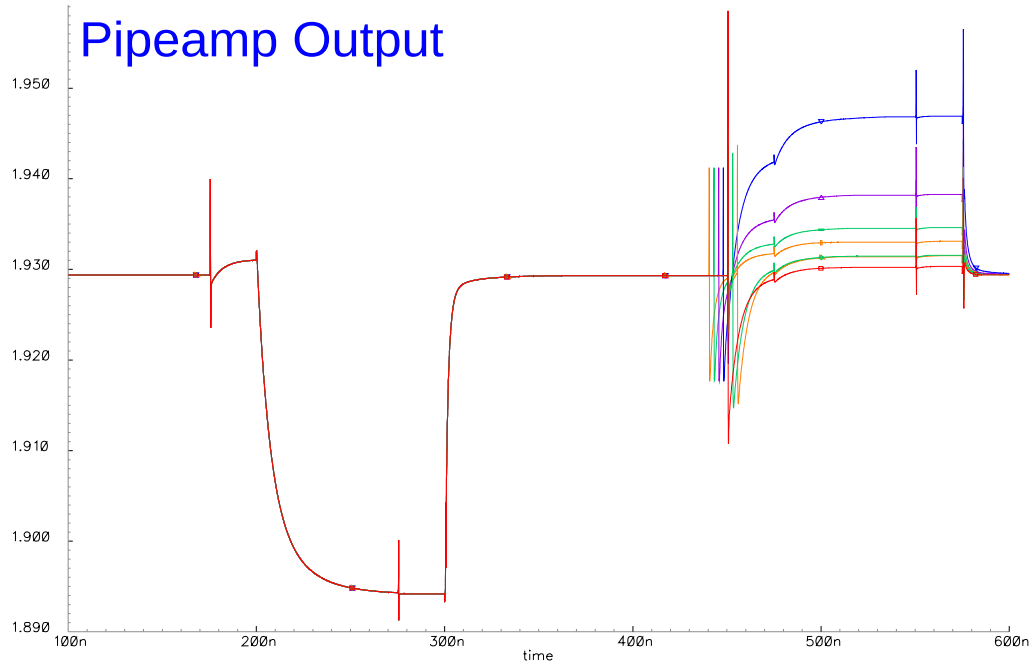

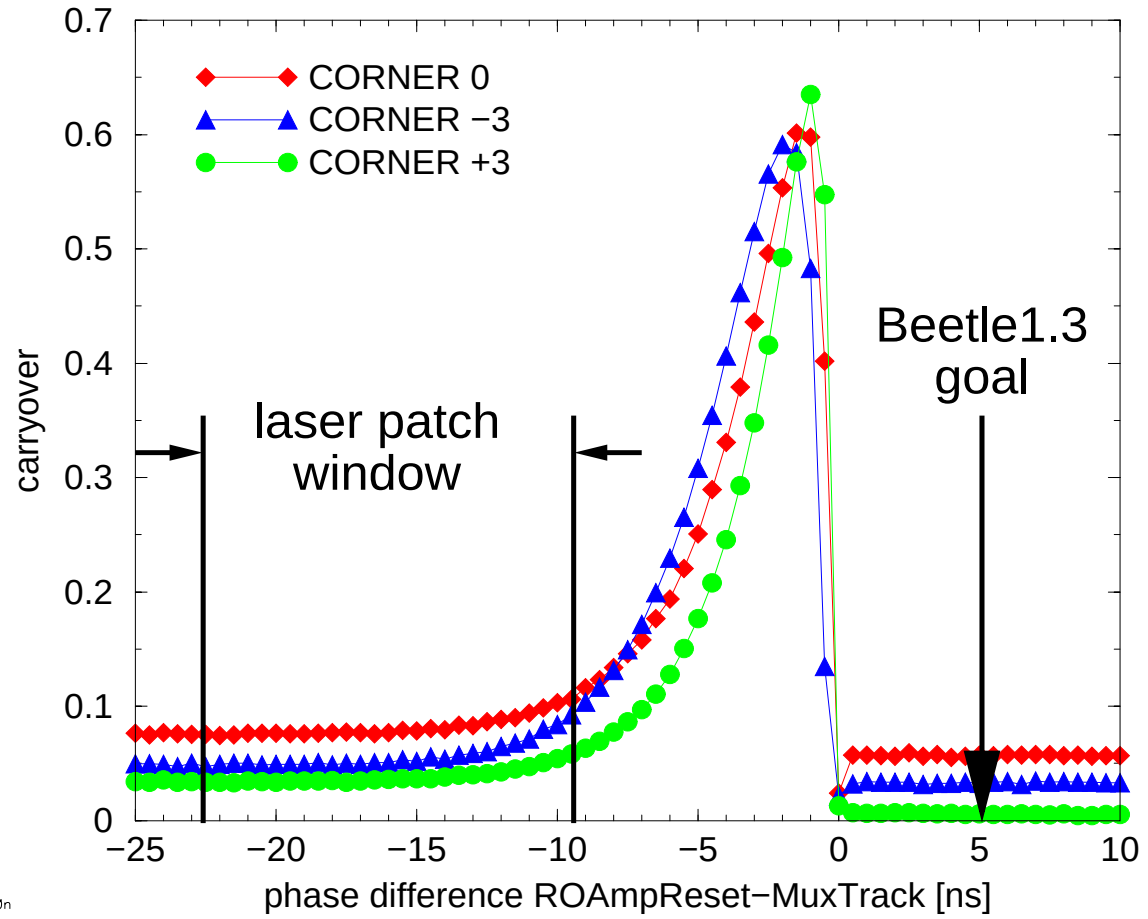

Modification in Beetle1.3: analog delay of MuxTrack by 5 ns

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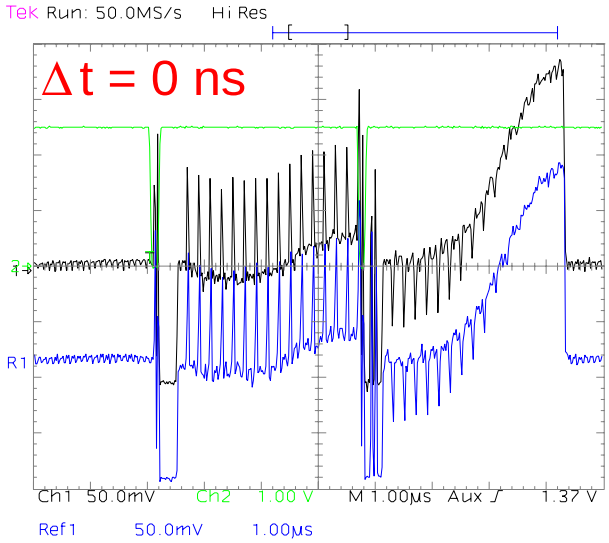
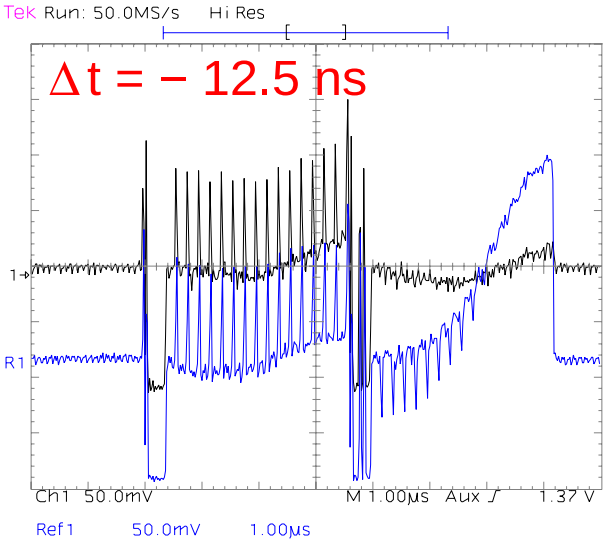
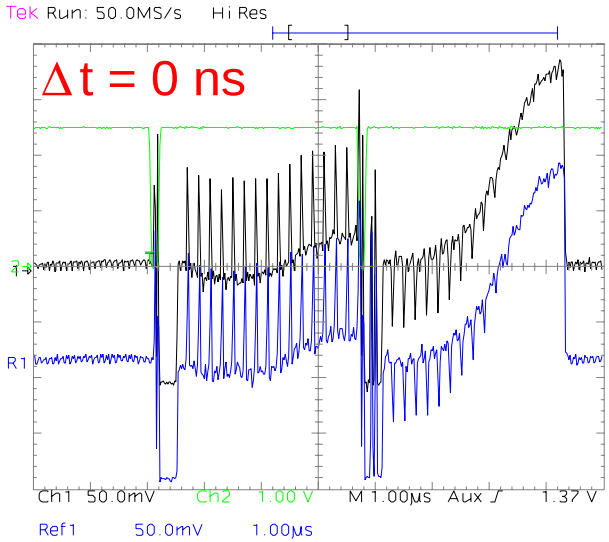
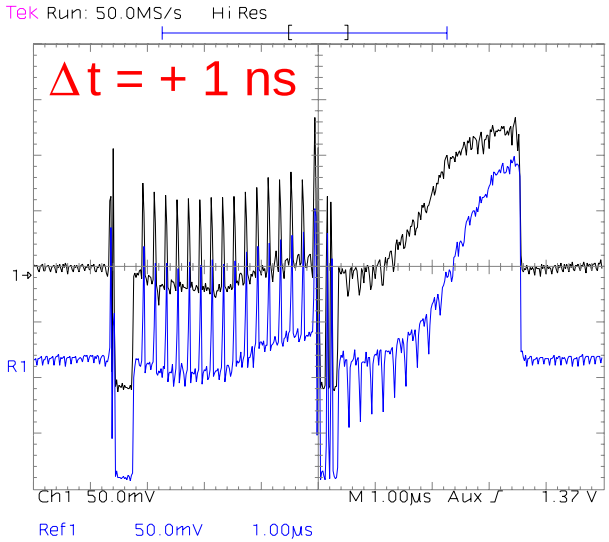
Sticky Charge Effect (4)

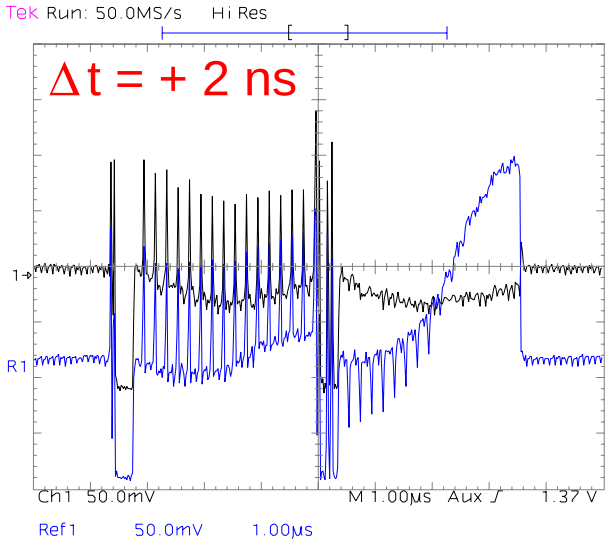
probe needle test with pos. and neg. phase shift











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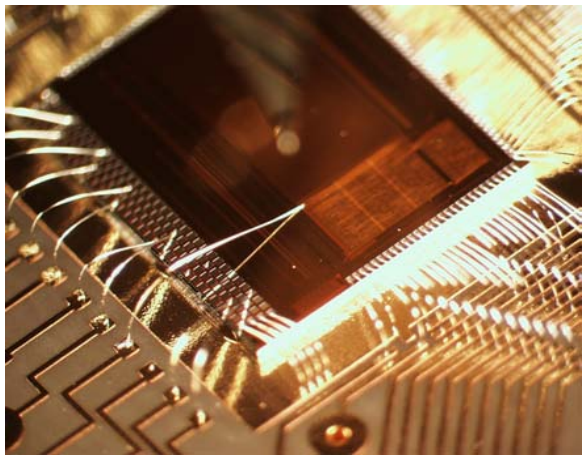
80 MHz X−talk

cross talk with a frequency spectrum of 80 MHz

present on

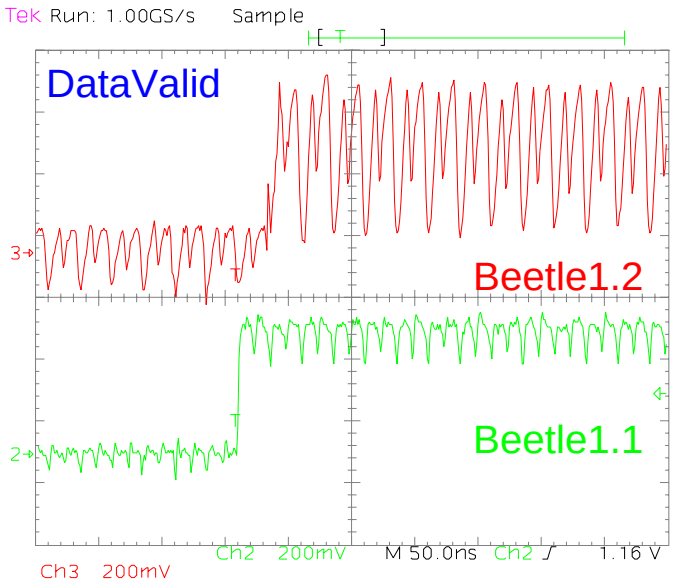
- digital signals, e.g. DataValid
- analogue signals, e.g. AnalogOut
- power supply lines: Vddd, Vdda

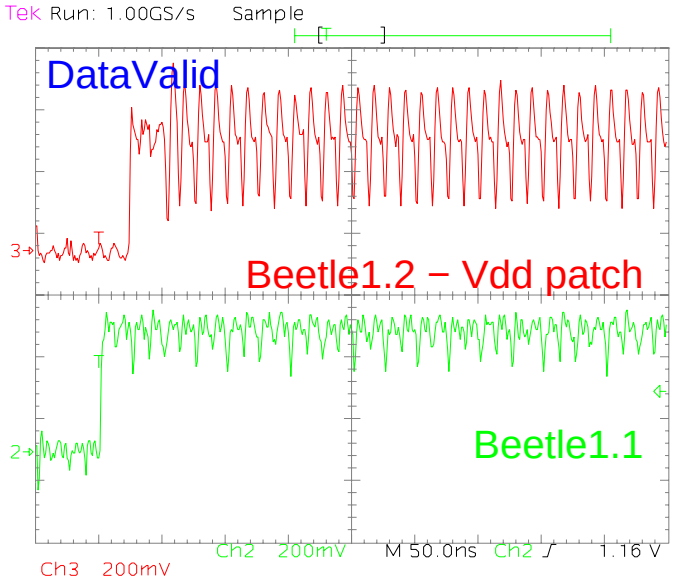
comparison:	Beetle1.1	Beetle1.2
# flip−flops:	1349	3043
# clock buffers:	21	284
guard rings logic core:	analogue	digital



Possible solutions:

- reduced no. of clock buffers
- on−chip power blocking





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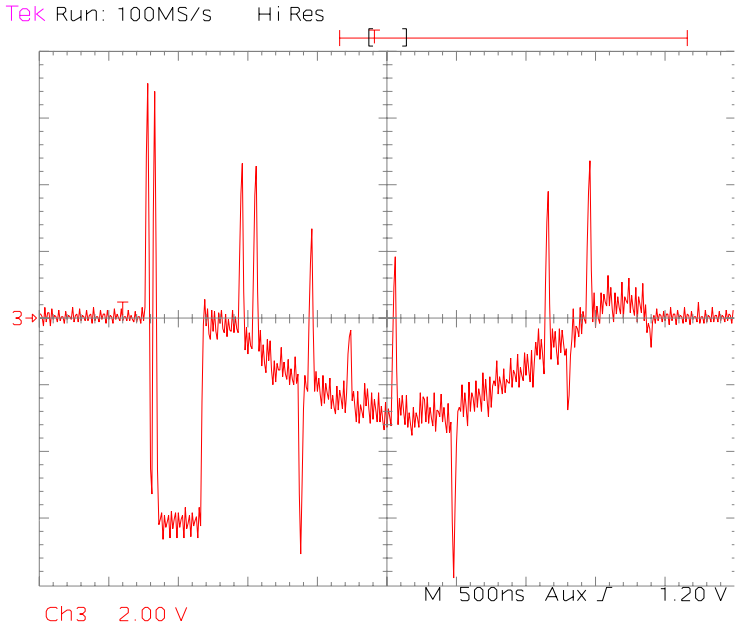
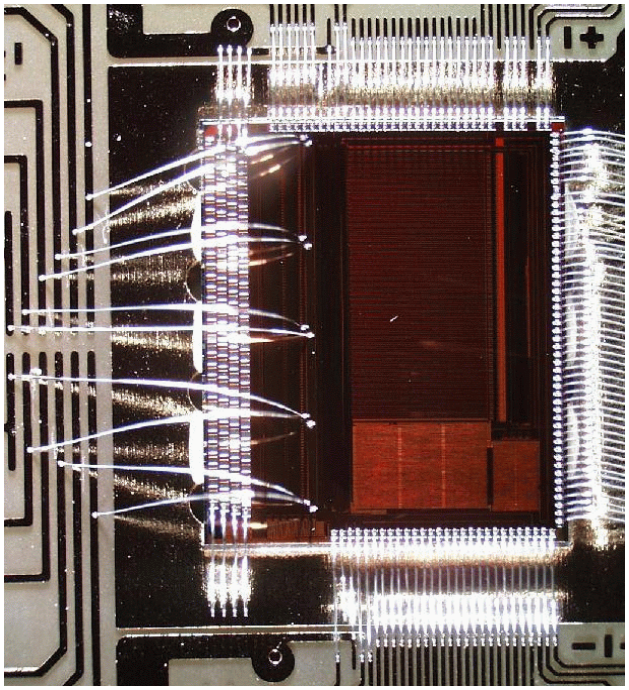
Readout Baseline Variation

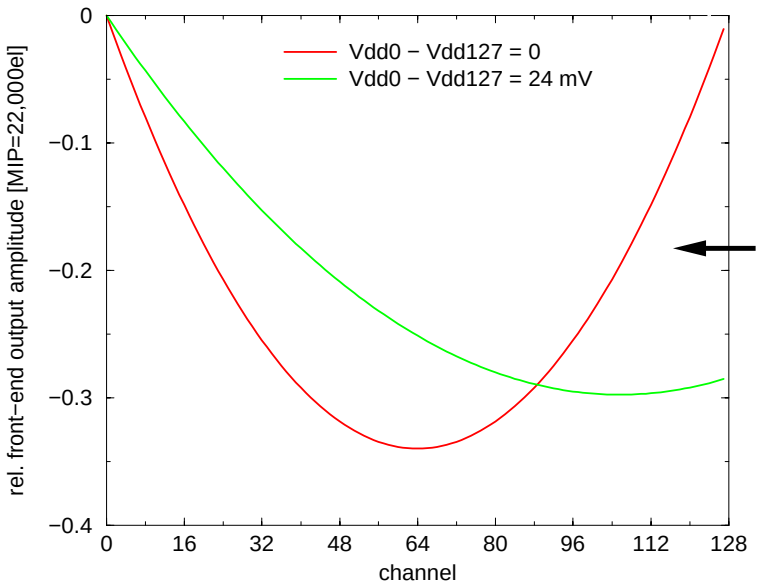


Observation:
shaper bias current affects
amplitude of baseline variation

Laser Patch: →
probing shaper power supply
at various channels

Beetle Surgery





difference in VDD between
ch.0 and ch.127: 24 mV

← Simulation:
resistive VDD−network in shaper

Modification in Beetle1.3: additional power supply lines in shaper (+ 100 um)

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Comparator Changes

Motivation: offset−spread: σ = 2.4 DAC units = 300 nA = 0.2 MIP

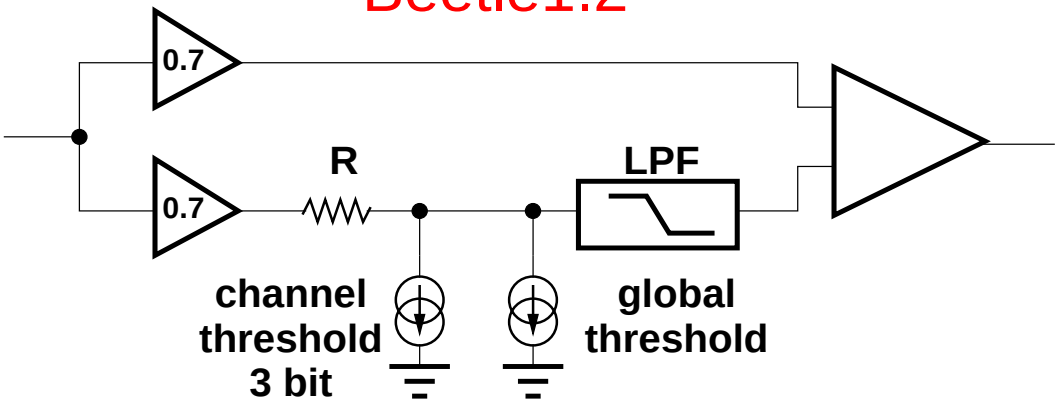
- bipolar
- too large for compensation with present DACs for channel threshold

Measures:

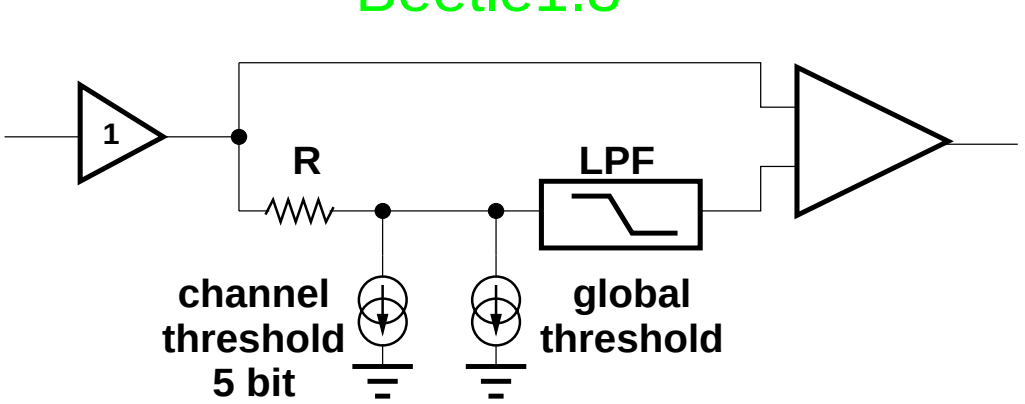
- merging input buffers: reduces additional offset
- gain increase of buffer: reduces influence on offset
- increase resolution of threshold current to 5 bits

  required: ±900 nA = ±0.6 MIP

Beetle1.2



Beetle1.3



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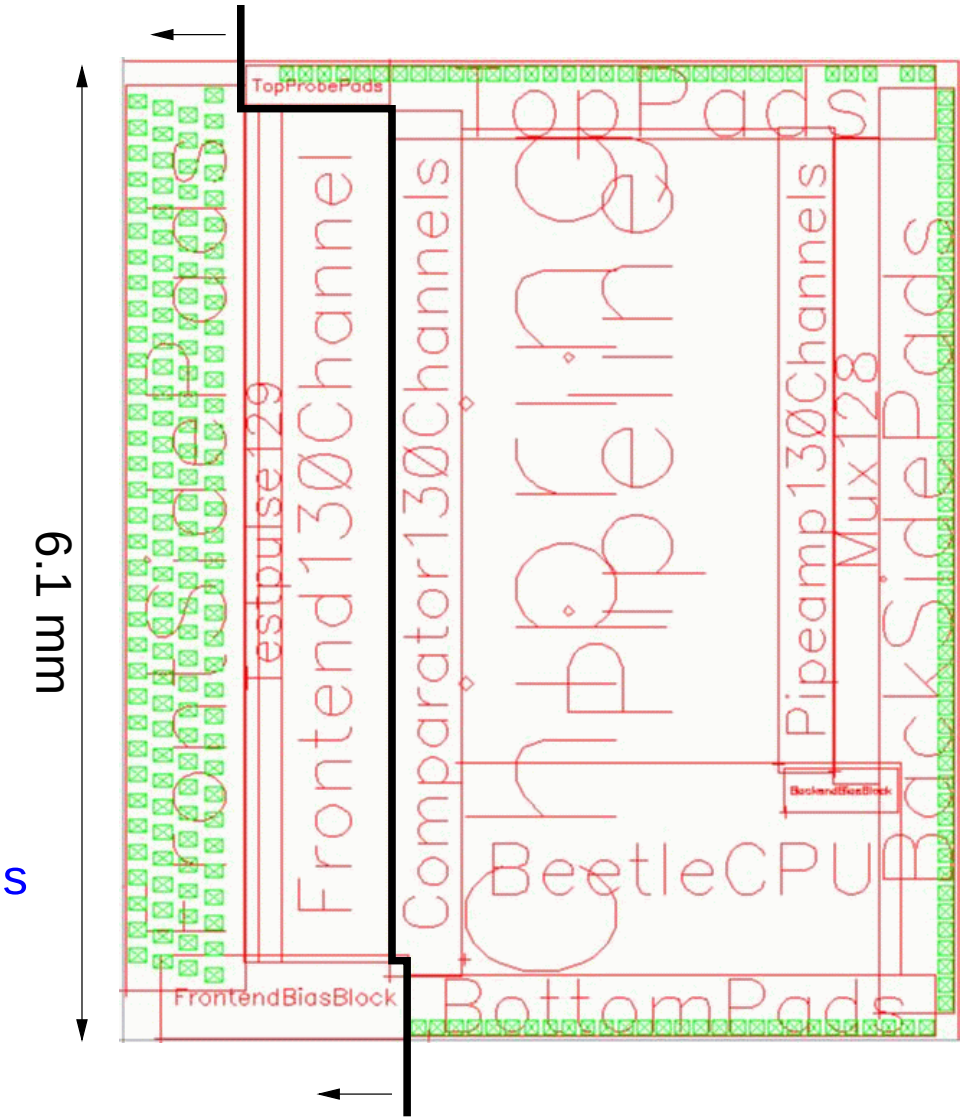
Chip Size

- Beetle1.0/1.1: (5.4 x 6.1) mm2
- Beetle1.2: (5.1 x 6.1) mm2
  modified layout of protection diodes
  of analogue input pads
- Beetle1.3: (5.3...4x 6.1) mm2
  - ◇ comparator resolution increases by 2 bits
  - ◇ additional power lines for shaper

enlargement of chip size
- is limited to one dimension
- only affects position of analogue input pads



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Outline: Further Issues

- DACs: Radiation Hardness
- Test Pulse Generation
- Overvoltage Problem
- Corner Simulation

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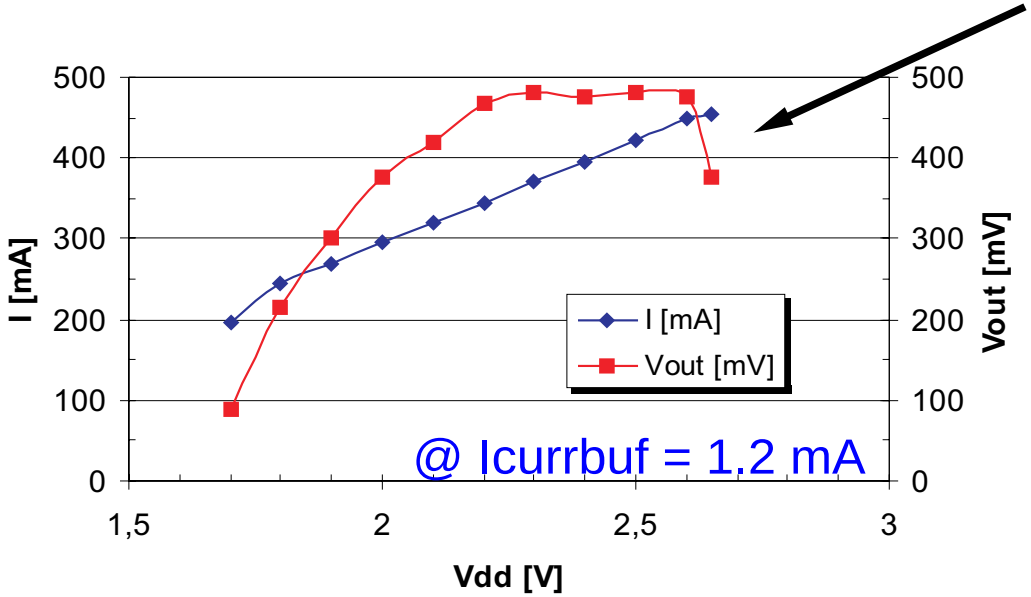
Stress Test on Beetle1.2

reported on Beetle Review in January 2003: problem of Beetle1.2 @ Vdd > 2.5 V (2.6...2.7 V)



Solved !

- high bias current of output buffer (Icurrbuf) generates destructive current density
- increasing receiver series resistance allows reduction of Icurrbuf at the same output gain

stress test on Beetle1.2 @ Icurrbuf = 100 uA: 12 hours @ 3.3 V without problems

in Beetle1.3: limitation of current density in output buffer

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Modifications in Beetle1.3

- 5 V compatible I2C−Pads
- analogue delay of MuxTrack signal: fix of sticky charge effect
- improved comparator: 5 bit threshold resolution; increases chip length by 100 um!
- improved shaper power routing: increases chip length by 100 um!
- improved pipeamp power routing (already on Beetle12MA0)
- separation of power supply of multiplexer and logic core
- separation of comparator LVDS pad power
- modified front−end power pads (power and ground at top and bottom of chip)
- introduction of bias generator probe pad
- modified test pulse pattern: uniform amplitude
- merged pad openings of adjacent power pads
- on−chip power blocking
- limitation of current density in output buffer (to avoid overvoltage problem)
- fix of daisy chain bug
- fix of Rclk−divider bug: re−synthesis + place and route

- done
- under work
- to be done

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