

# Status of the



# Chip

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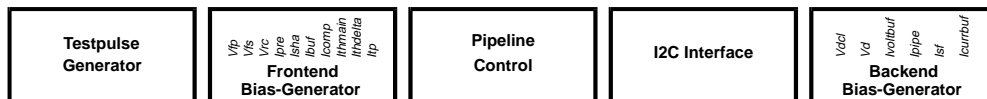
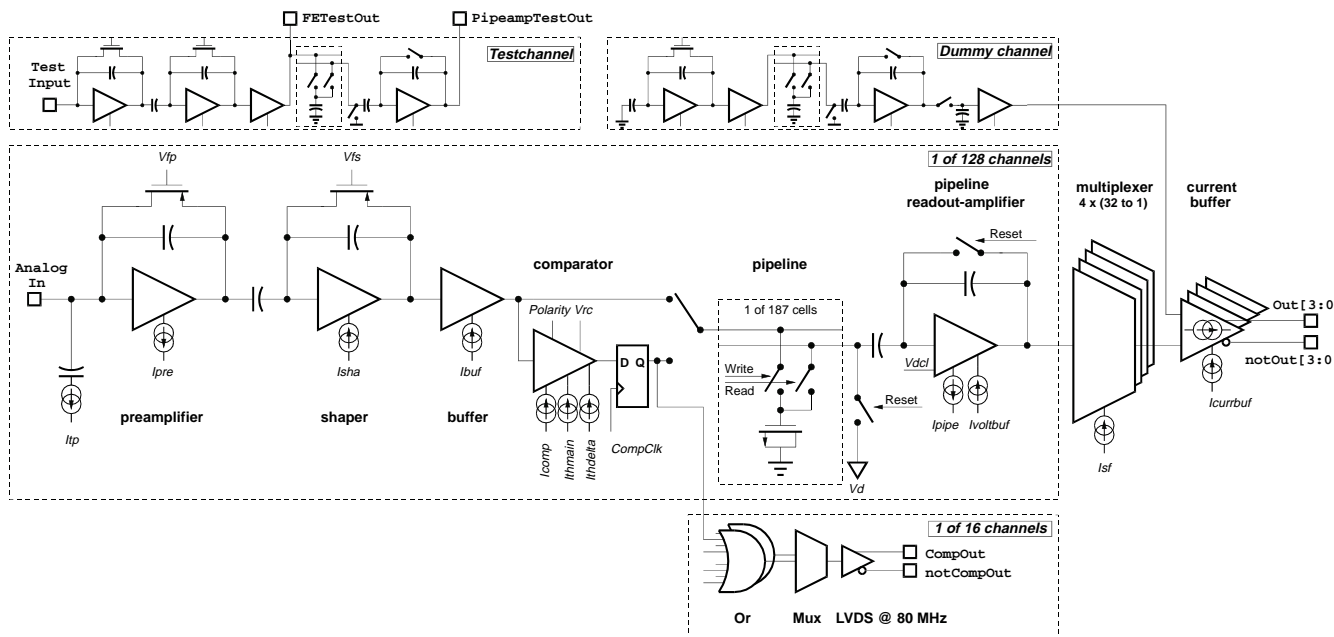
# What is Beetle?

## Features:

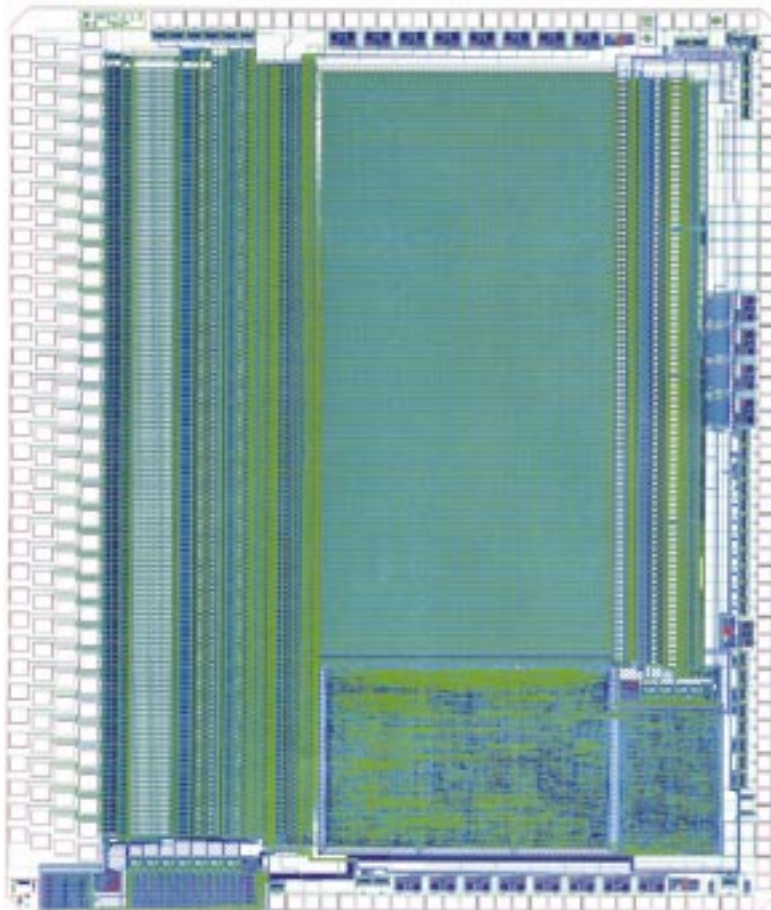
- 128 input channels
- CSA/Shaper with 25ns peaking time
- 40 MHz sampling (LHC clock)
- 128 discriminators with switchable polarity
- analogue memory for 160 sampling steps
- buffer for 16 triggered events
- ➔ 4  $\mu$ s max. latency
- ➔ 900ns/event readout speed
- internal DACs for bias settings
- test pulse injector with adjustable amplitude
- setup/slow control via I<sup>2</sup>C interface

## Employment in LHCb:

- VELO
- Pile-up veto counters
- Silicon Tracker
- RICH (in case of MAPMTs)



# Beetle: Layout & Key Requirements



| environment |                          |               |   |
|-------------|--------------------------|---------------|---|
| 1.1         | total radiation dose     | 10 Mrad       | ✓ |
| 1.2         | average dose rate        | 0.2 rad/s     | ✓ |
| 1.3         | max. capacitive load     | 30 pF         | ✓ |
| 1.4         | max. load variation/chip | 10 pF (?)     | ✓ |
| 1.5         | max. occupancy           | 5 %           | ✓ |
| 1.6         | temperature range        | - 30 to +60 C | ✓ |

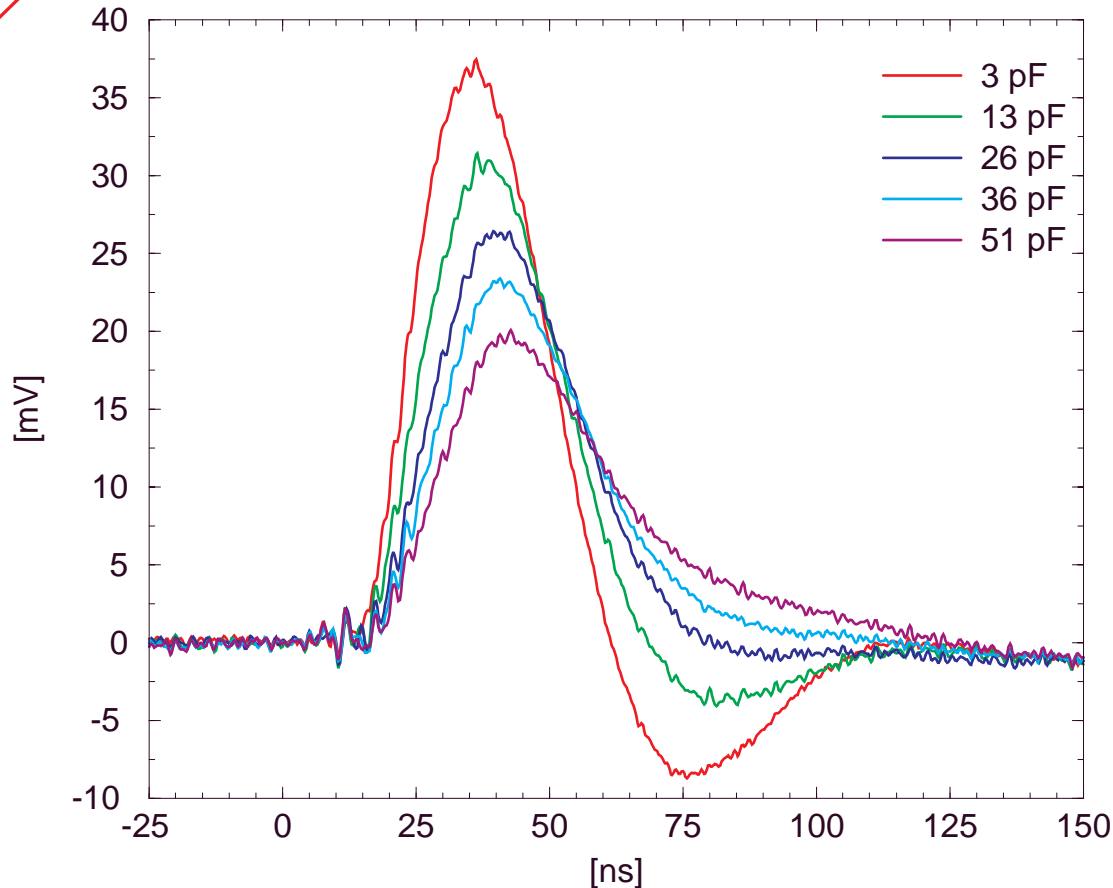
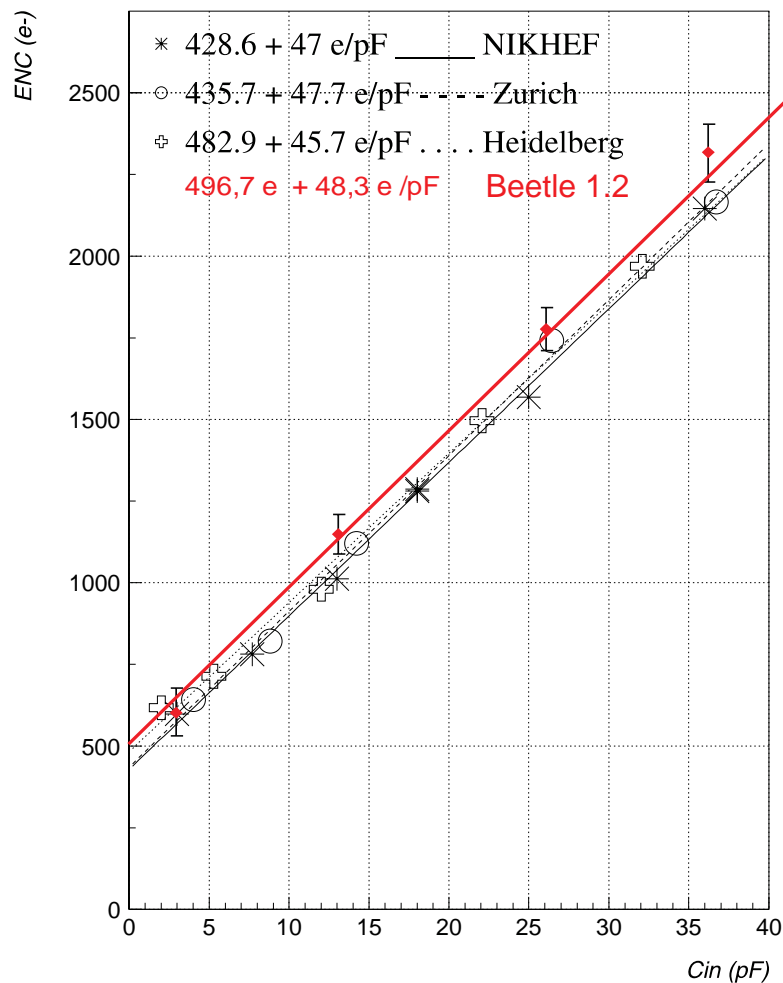
| DAQ requirements |   |             |   |
|------------------|---|-------------|---|
| 2.1              | sampling frequency                        | 40 MHz      | ✓ |
| 2.2              | max. L0 latency                           | 4 $\mu$ s   | ✓ |
| 2.3              | L0 accept rate                            | 1 MHz       | ✓ |
| 2.4              | consecutive triggers                      | yes         | ✓ |
| 2.5              | trigger buffer                            | 16 triggers | ✓ |
| 2.6              | max. readout time                         | 900 ns      | ✓ |
| 2.7              | registers read-back to ECS                | yes         | ✓ |
| 2.8              | fast reset of pipeline and fifo           | yes         | ✓ |
| 2.9              | differential inputs for trigger and clock | yes         | ✓ |

| basic VELO requirements |   |                     |     |
|-------------------------|---|---------------------|-----|
| 3.1                     | max.total power consumption/channel       | 6 mW                | ✓   |
| 3.2                     | max.peaking time                          | 25 ns               | ✓   |
| 3.3                     | max.pulse spill over after 25 ns          | 30 %                | ✓ ? |
| 3.4                     | max.non-linearity over $\pm 110,000 e^-$  | 5%                  | ✓   |
| 3.5                     | max.cross talk between channels           | 5%                  | ✓   |
| 3.6                     | max.total ENC at 10 pF capacitive load    | 1500 e <sup>-</sup> | ✓   |
| 3.7                     | min.tolerable input current               | 20 nA               | ✓   |
| 3.8                     | min.output driving strength at 100 Ohm TP | 1 m                 | ✓   |
| 3.9                     | min.chip yield                            | 30%                 | ✓   |
| 3.10                    | synchronization check with PCN            | yes                 | ✓   |

? but X-talk to next readout (sticky-charge)

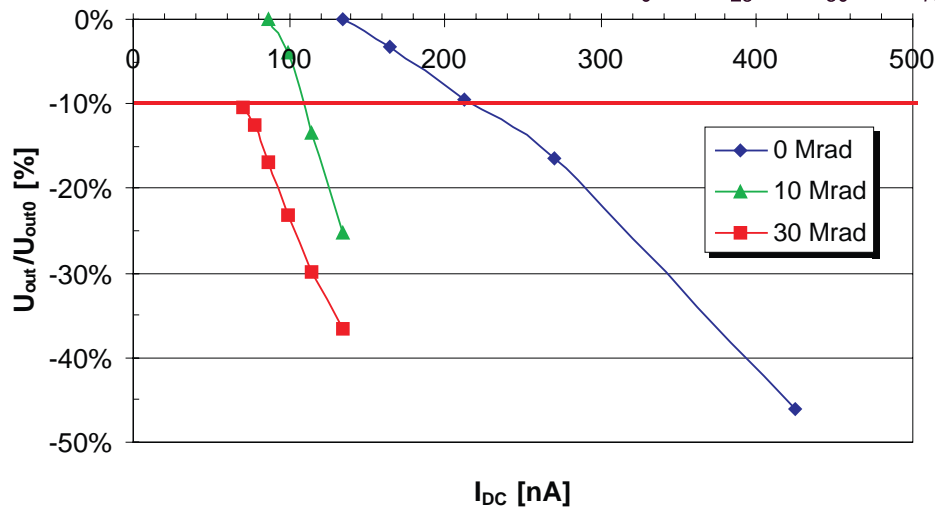
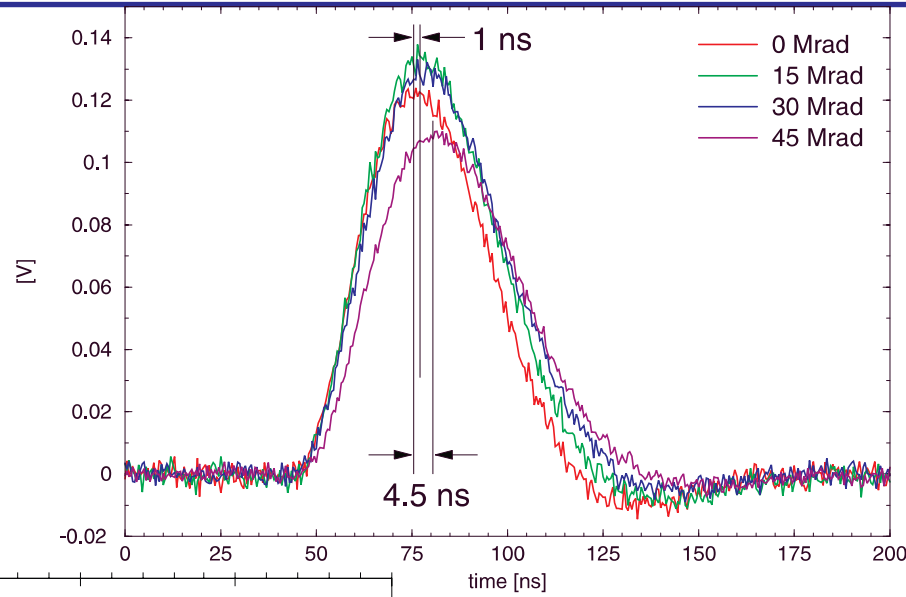
No Specification Document for VETO counters yet, but threshold variation too large to compensate with channel DACs

# Beetle: Pulse Shape & Noise



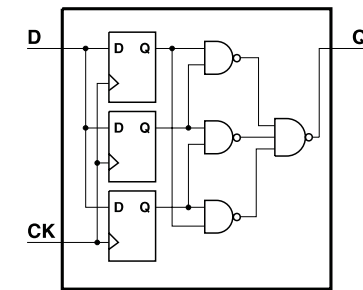
# Beetle: Radiation Hardness

## TID Effects

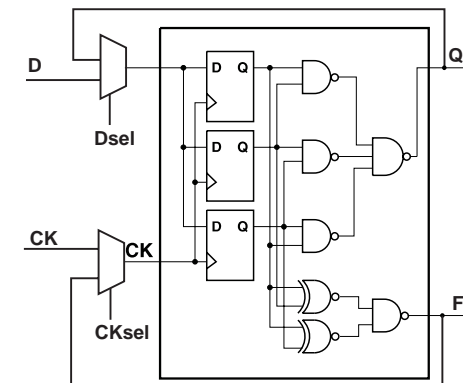


## SEU Protection

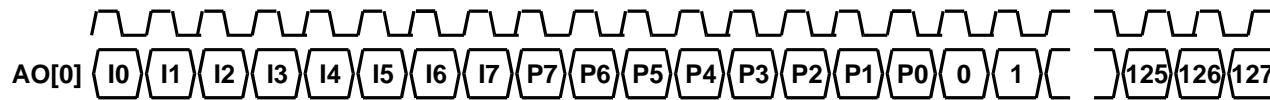
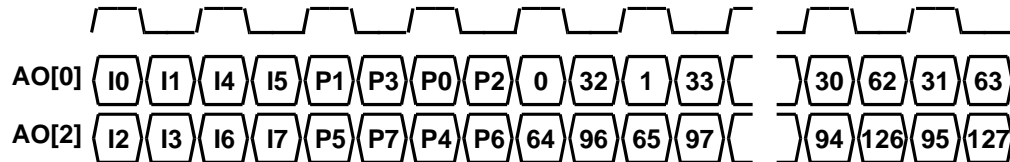
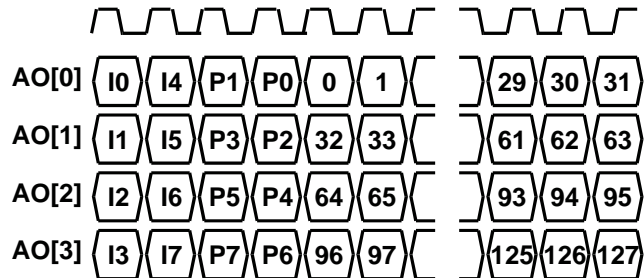
State machines



Static registers

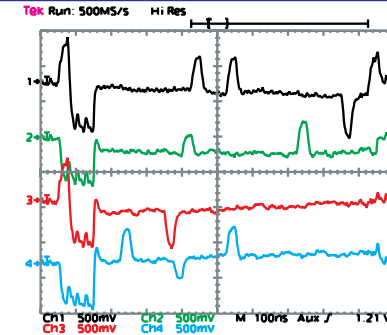


# Beetle: Readout Modes

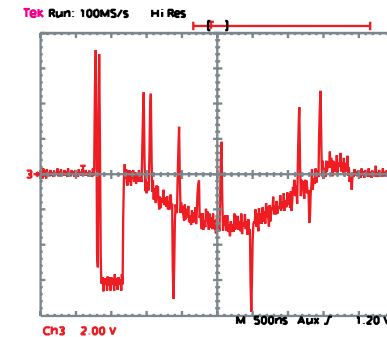


| Bit   | Description  |
|-------|--|
| I0    | Start Bit: Always 1                                      |
| I1    | (even) parity of pipeline column number (PCN)            |
| I2    | ActiveEDC: indicates active error correction logic (EDC) |
| I3    | parity of <i>CompChTh</i> register                       |
| I4    | parity of <i>CompMask</i> register                       |
| I5    | parity of <i>TPSelect</i> register                       |
| I6-I7 | 2 LSB of <i>SEUcounter</i> register                      |
| P0-P7 | Pipeline column number (PCN)                             |

VeLo/ST

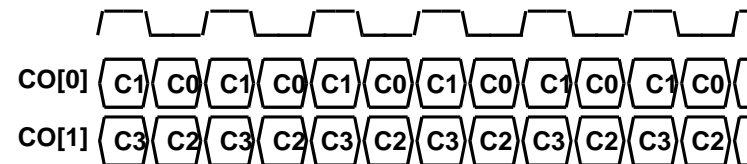


RICH



Lab

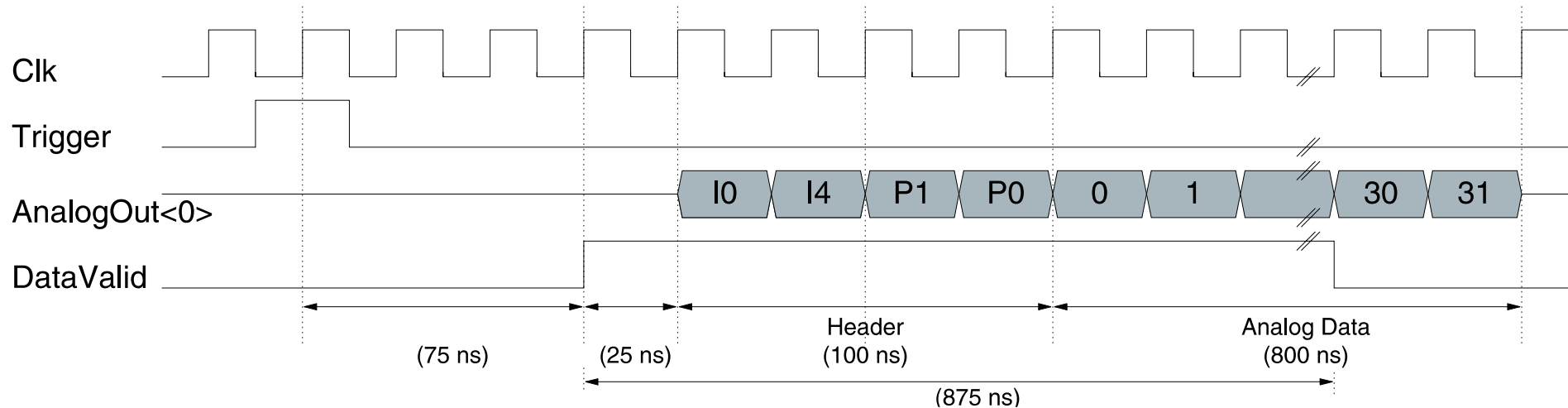
Comparator  
(Veto counters, prompt binary readout)



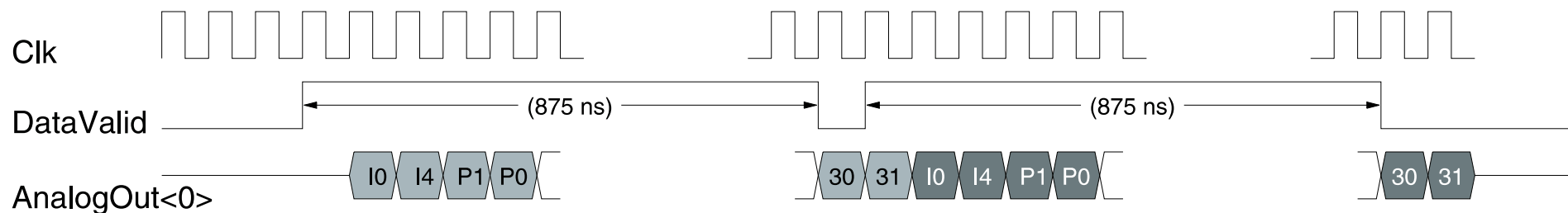


# Beetle: Readout Timing

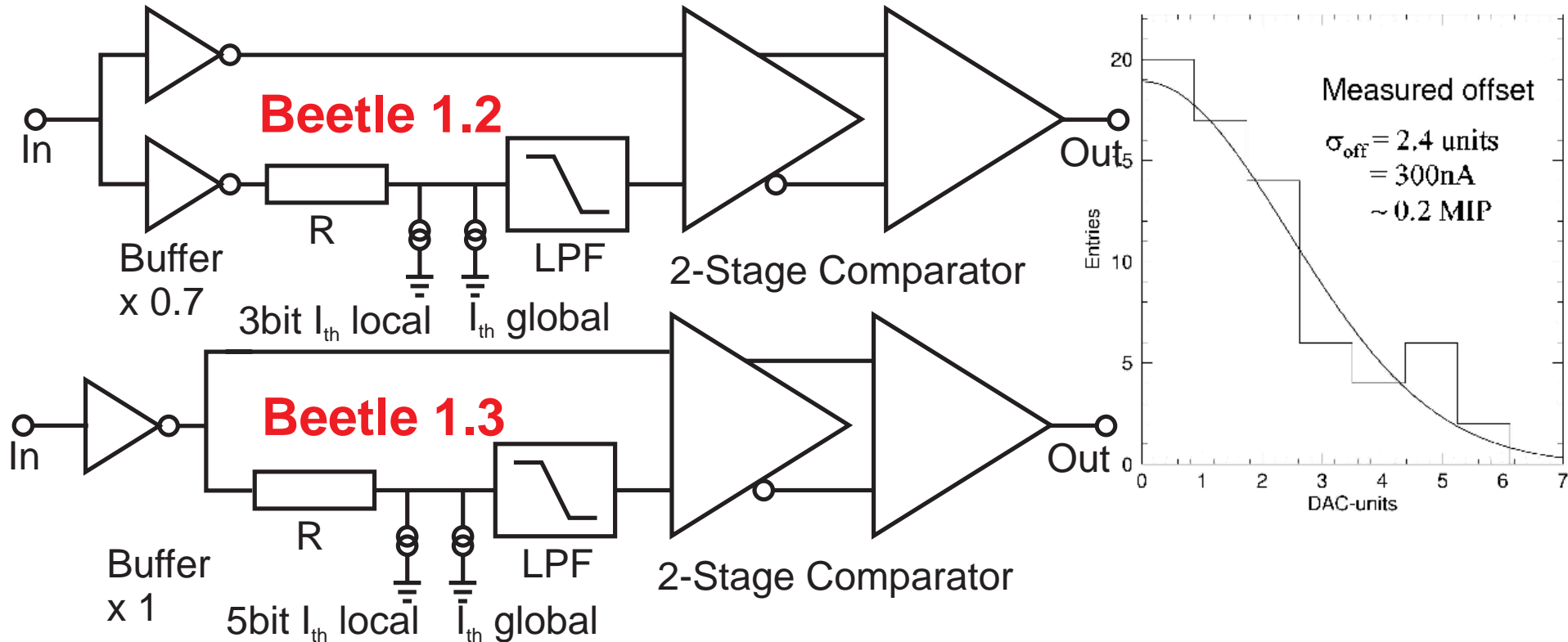
## Single Readout



## Consecutive Readout



# Discriminators and Offsets



**Measured offset:  $\sigma_{\text{offs}} = 300\text{nA} = 0.2\text{MIP}$**

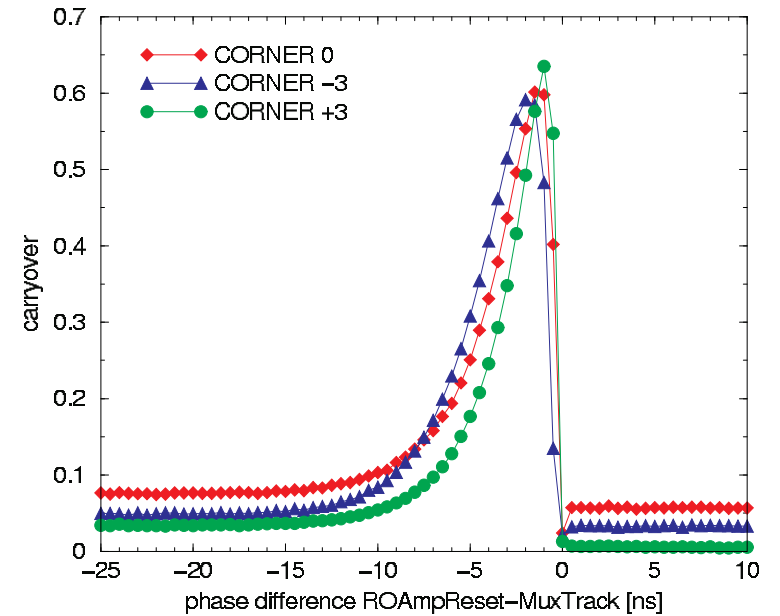
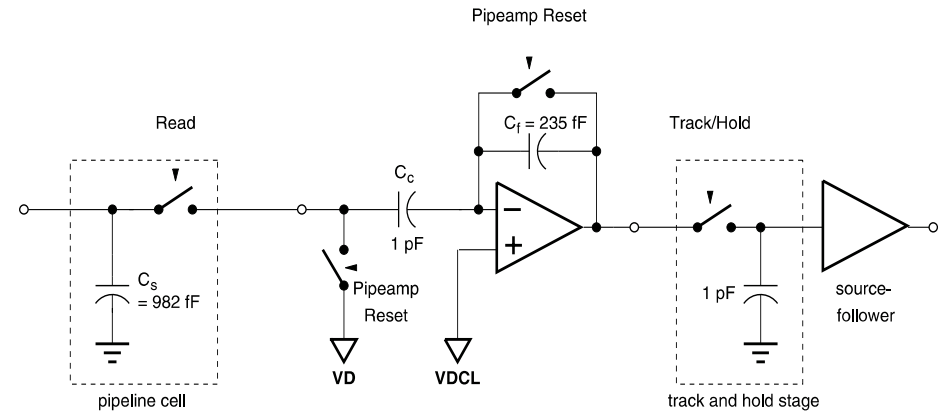
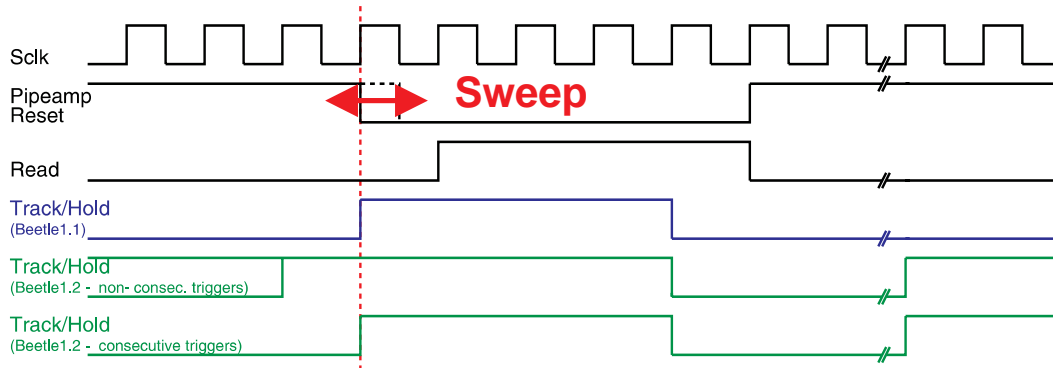
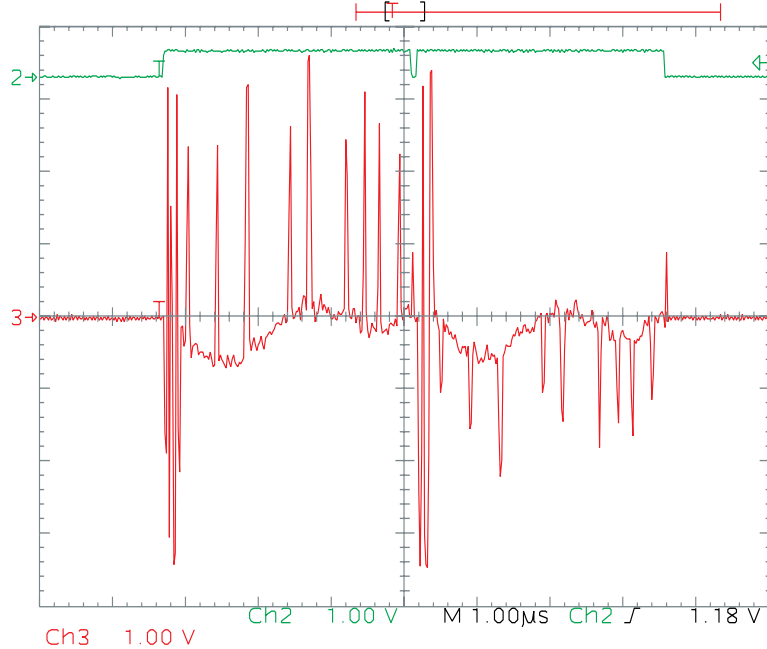
**bipolar and too large for compensation with local DACs**

- consistent with simulation ( $\sigma_{\text{offs}} = 350\text{nA}$ ,  $100\text{nA}$  from  $\Delta L$ ,  $335\text{nA}$  from  $\Delta V_{\text{th}}$ )
- ➔ compensation requires  $\pm 0.6$  MIP =  $\pm 900$  nA local DAC range
- ➔ a single x1 buffer will reduce the absolute offset value and it's influence by an increased gain



# Sticky Charge Effect

Tek Run: 50.0MS/s Hi Res



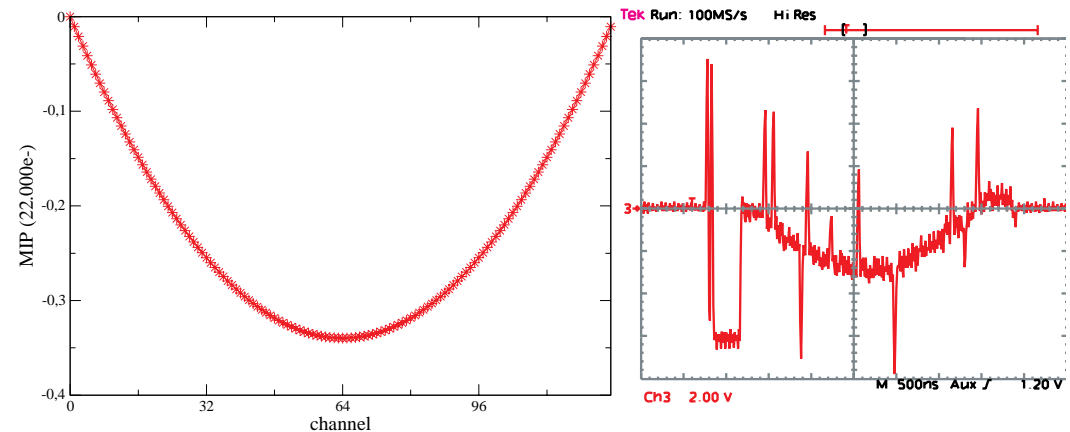
# Other Issues

## 80MHz crosstalk

- Spikes with a large Amplitude on the readout lines have been observed
- They're also present on the Vdd supply lines
- Not on Vss or logic "low" outputs
- Not on Beetle 1.1

Possible sources:

- # of FlipFlop increased by 2.2 on Beetle 1.2
  - 1356 in fast control
  - 279 in slow control
  - 384 in MUX
  - 1024 static registers
- # of clock buffers drastically increased:
  - Beetle 1.1 ~ 20 Clk-Buffers
  - Beetle 1.2 ~ 275 Clk-Buffers
  - OTIS 1.0 ~ 80 Clk-Buffers
- Layout issues



## Bent Baseline

- shape of the readout baseline is that of a clothesline in 128 ch mode

Reason:

- Voltage drop on the shaper power supply lines
- (ohmic resistance)
- Preamp, buffer and mux are not affected (AC-coupling & source followers)
- Gain drop due to this is <1%

# Modifications for Beetle 1.3

- modified power supply lines in PipeAmp (from Beetle 1.2 Ma0)
  - Improved comparator made by Hans Verkoojen
  - Separation of digital power supplies for MUX and core (FC)
  - Different connectivity for FE power pads
  - Improved routing at rear side power pads
  - Probe-pads for front end bias
  - 5V compliant I<sup>2</sup>C interface
  - On-chip blocking capacitors
  - Fix of “sticky charge” problem (timing of PipeAmp control signals)
  - modified power supply lines in shaper (bent baseline)
  - Improved routing of core power supplies
  - Fix of output driver overvoltage problem
  - Fix of daisy-chain signals (pull-down or logic?)
  - Change of Rclk-divider
- => 100...300 $\mu$ m length increase

- Beetle 1.3 tape out: 23.06.2003
- Beetle 1.3 production start: Q4/2003