

# Status of Beetle1.0

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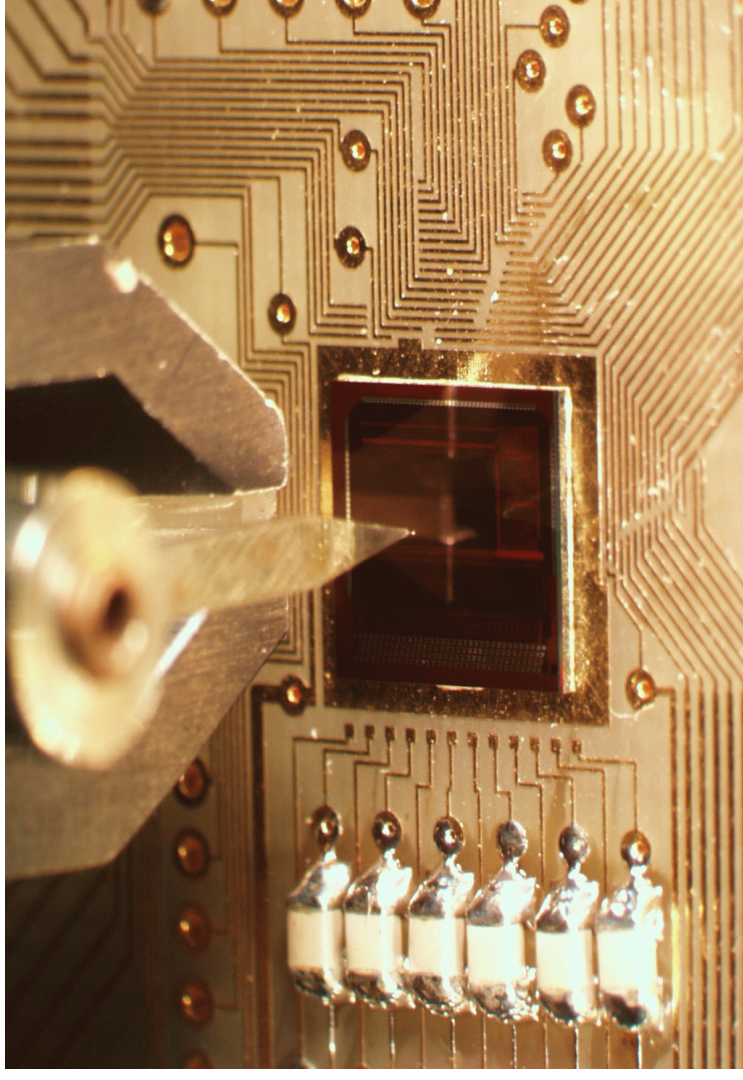
**Daniel Baumeister, Werner Hofmann, Karl-Tasso Knöpfle, Sven Löchner, Michael Schmelling, Edgar Sexauer**  
*(Max-Planck-Institute for Nuclear Physics Heidelberg)*

**Martin Feuerstack-Raible, Josef Schweda**  
*(University of Heidelberg)*

**Neville Harnew, Nigel Smale**  
*(University of Oxford)*

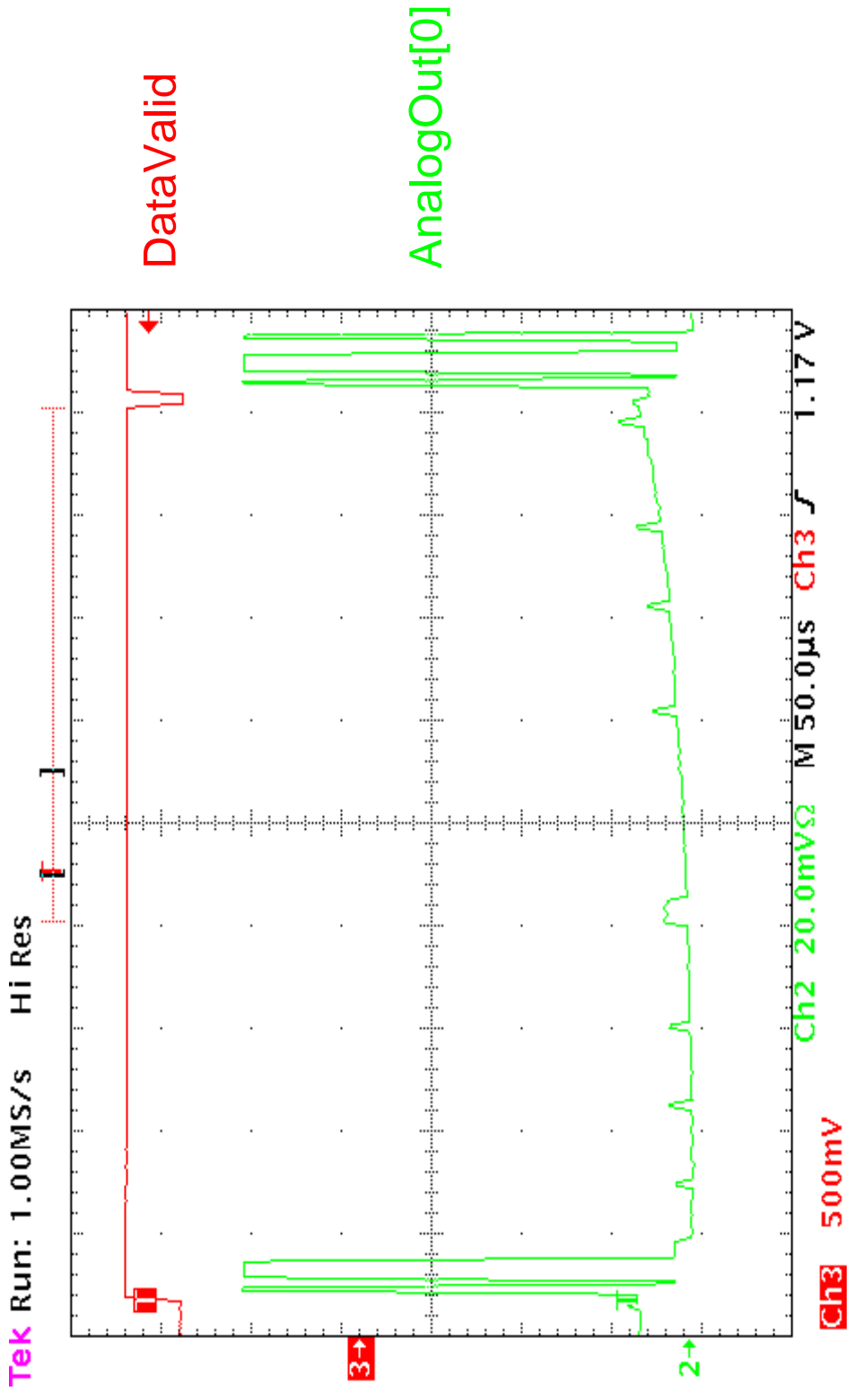
# Outline

- ◆ Principle Functionality of Beetle1.0
- ◆ Known Bugs
  - ◆ Tristate Buffer
  - ◆ Pipeline Readout Amplifier
- ◆ Performance
  - ◆ Complete Analogue Chain
  - ◆ Frontend Amplifier
  - ◆ Control Logic
  - ◆ Analogue Output Driver
- ◆ Future Plans



# Principle Functionality of Beetle1.0

## Readout Mode: 128 channels on 1 port (input signal on 11 channels)



# Bug in Tristate-Buffer

Tristate-Buffers control access to internal data bus

**Bug:** Diffusion shortcut to GND/VDD

(not recovered by checking software: diffusion is not extracted as a net!)

Bug causes internal data bus to be logic LOW:

Programming the chip has no effect !

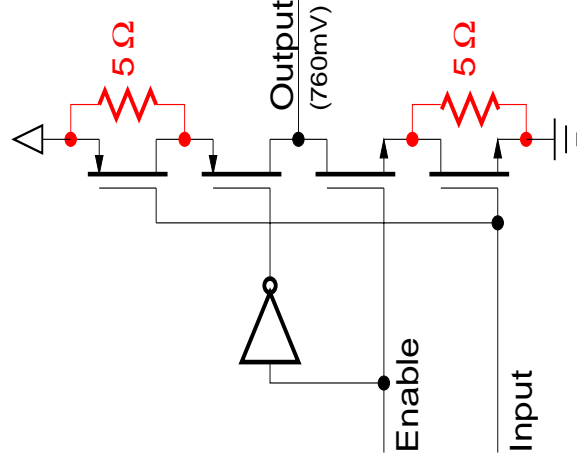
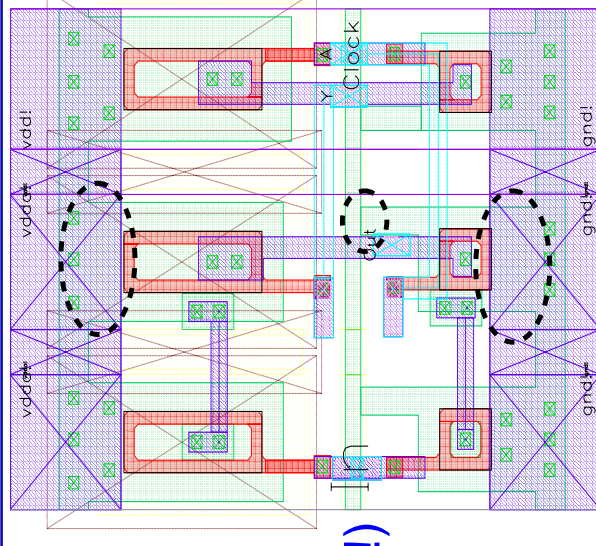
**Bug Fix:** Focused Ion Beam Patch (costs per chip: 3500 CHF)

After a patch: chip is programmable !

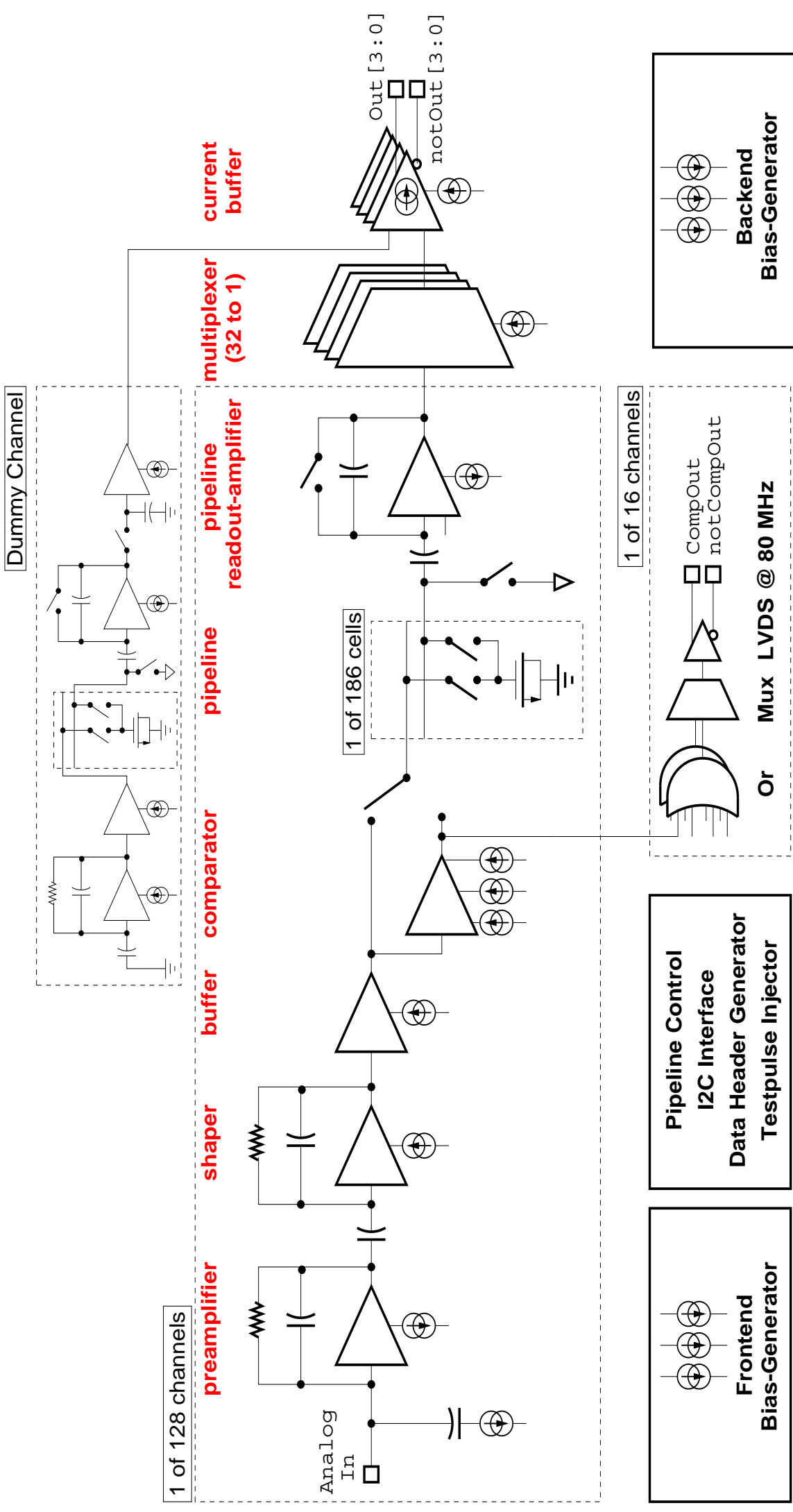
all registers are writeable via I2C-interface

reading of registers is not possible

**All further measurements have been done with patched chip!**

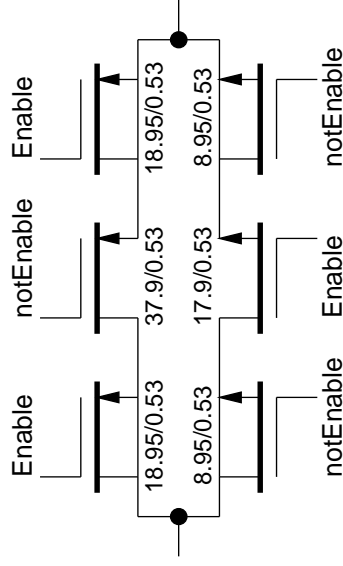


# Block Diagram of Beetle1.0

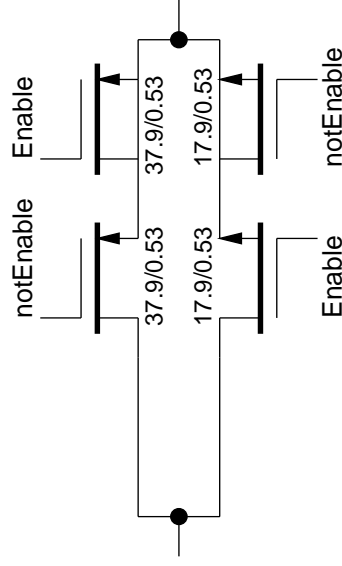


# Pipeamp: Bug in Transmission Gate

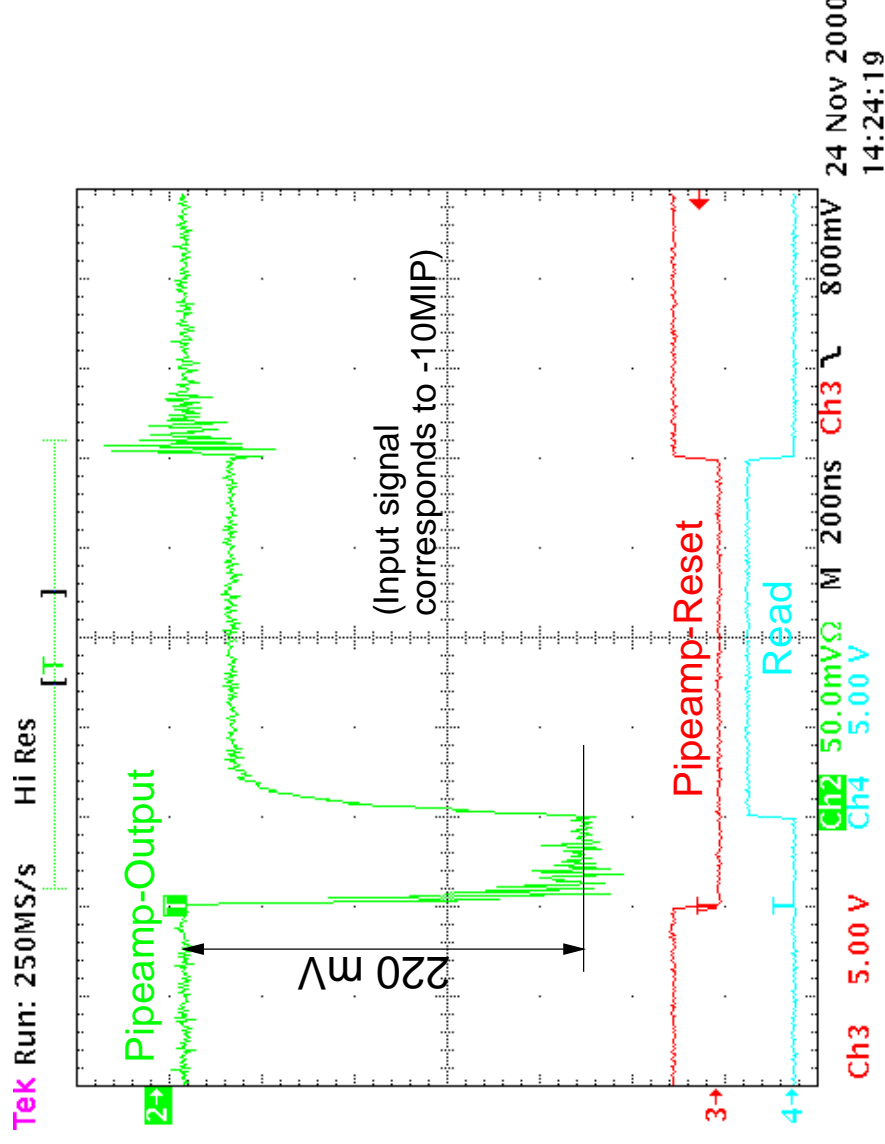
Transmission Gate  
as simulated



Transmission Gate  
corresponding to layout



## Measurement done on BeetlePA1.0

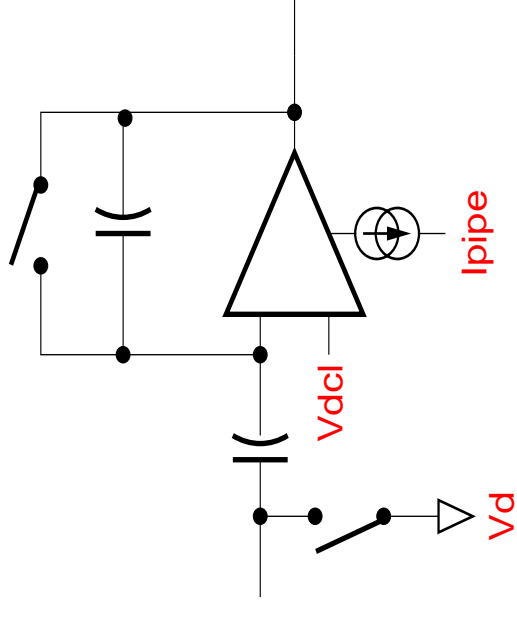
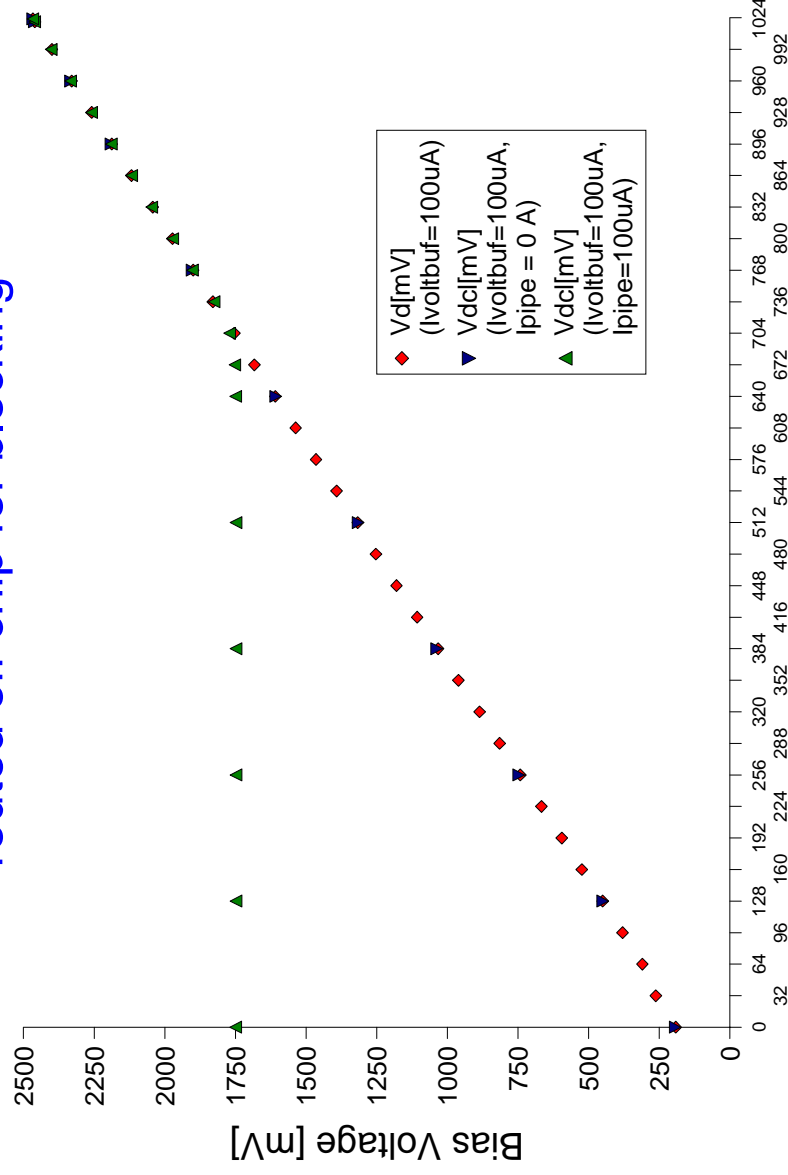


Voltage step can be reproduced in simulation!

# Pipeamp: Bug in Voltage Buffer

Pipeline Readout Amplifier needs two bias voltages:  $V_d$ ,  $V_{dcl}$

- ◆ buffered by a source follower
- ◆ routed off chip for blocking



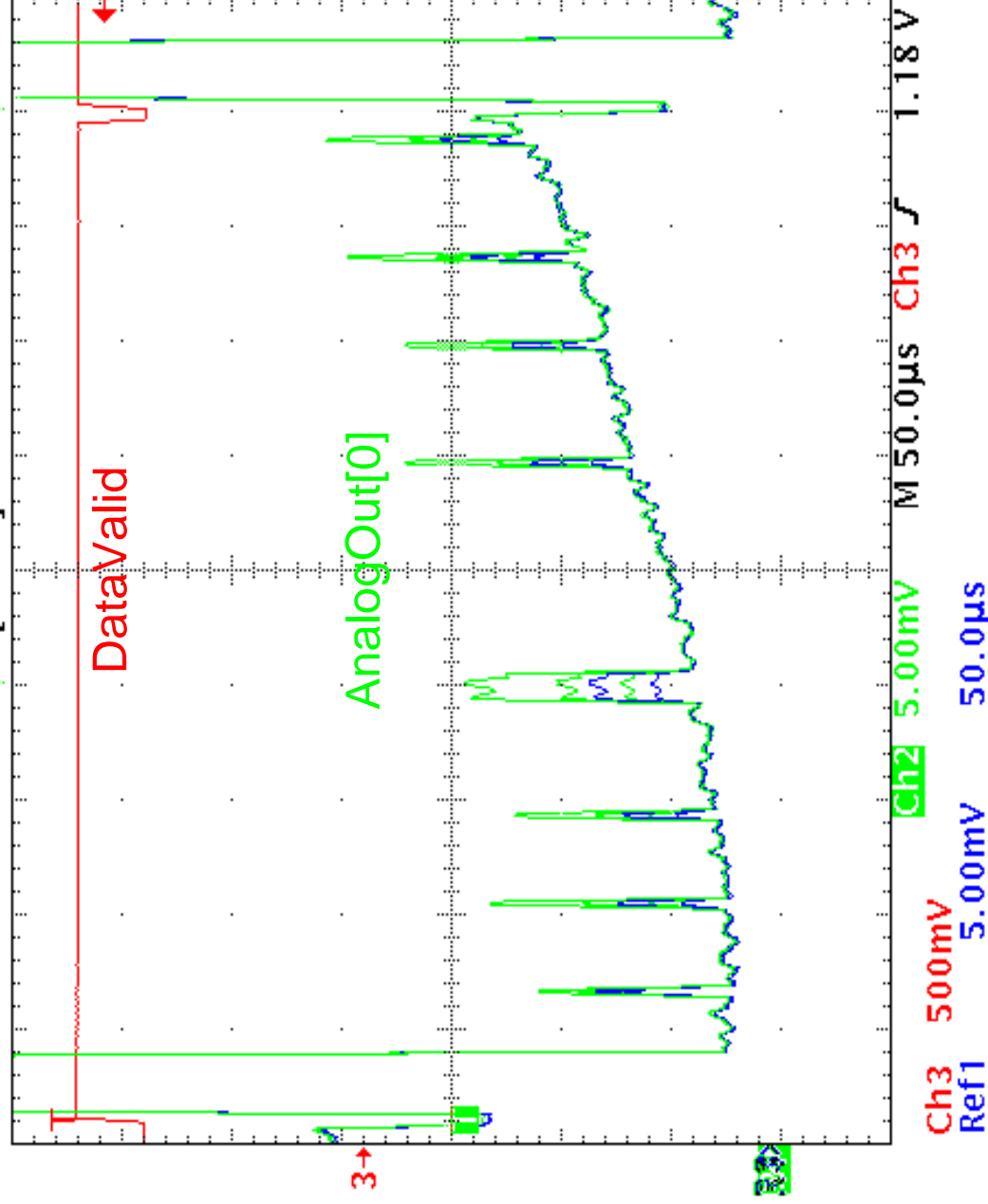
$V_{dcl}$ -Buffer is not able to drive bias current

Bug can be circumvented by external biasing

Register Content

# Analogue Output of Beetle1.0

Tek Run: 1.00MS/s Average



Readout Mode: 128 channels on 1 port

(Rclk=1/32 ScIk = 1.25 MHz)

Input signal on 11 channels

(8, 20, 32, 48-51, 80, 96, 108, 124)

Input charge corresponding to:

1 MIP, 2 MIP, 3 MIP, 4 MIP, 7 MIP

Simulated differential gain: 110  $\mu\text{A/MIP}$   
(6mV/MIP)

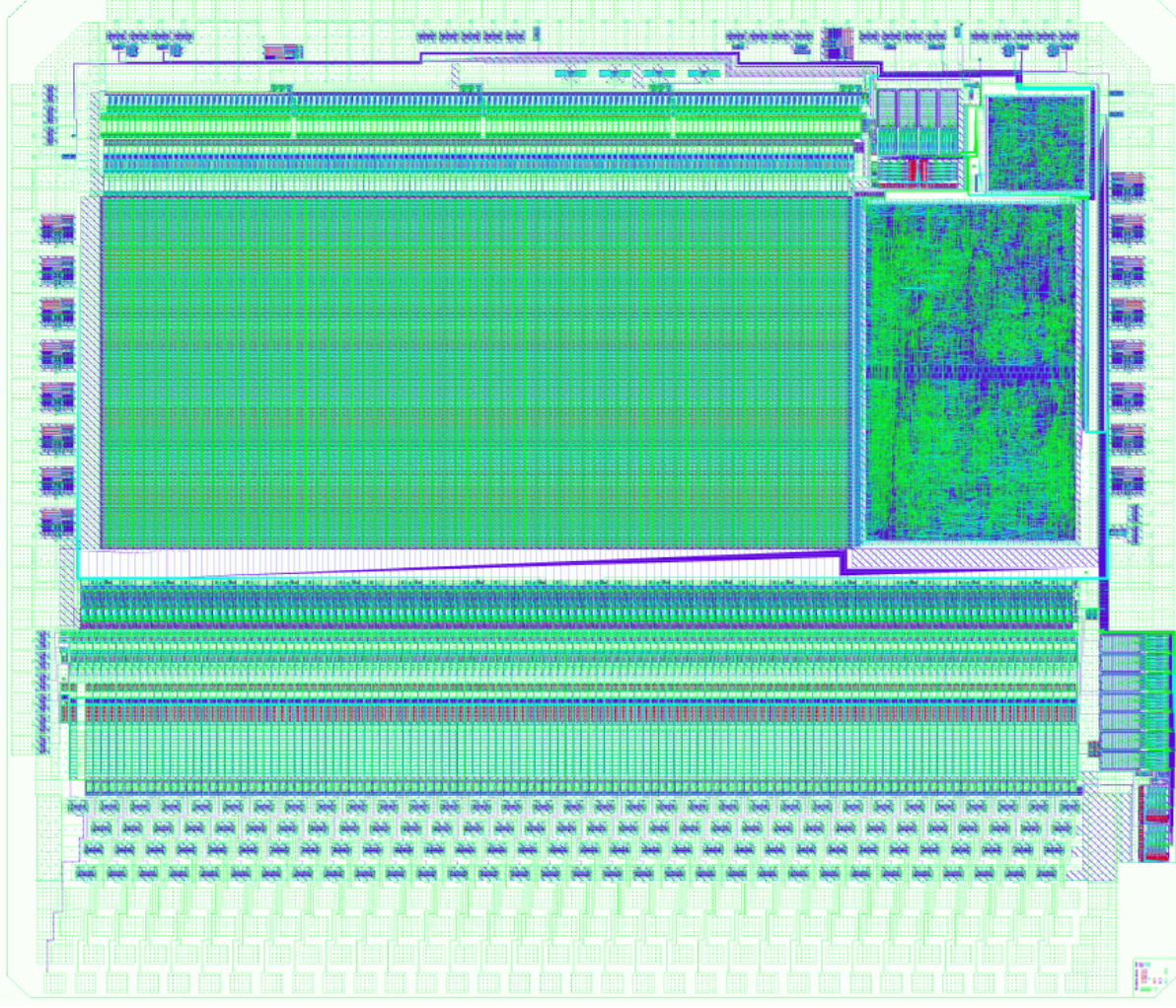
Measured differential gain: 26  $\mu\text{A/MIP}$   
(1.4mV/MIP)

Baseline-Shift:

voltage drop on Vdcl power line

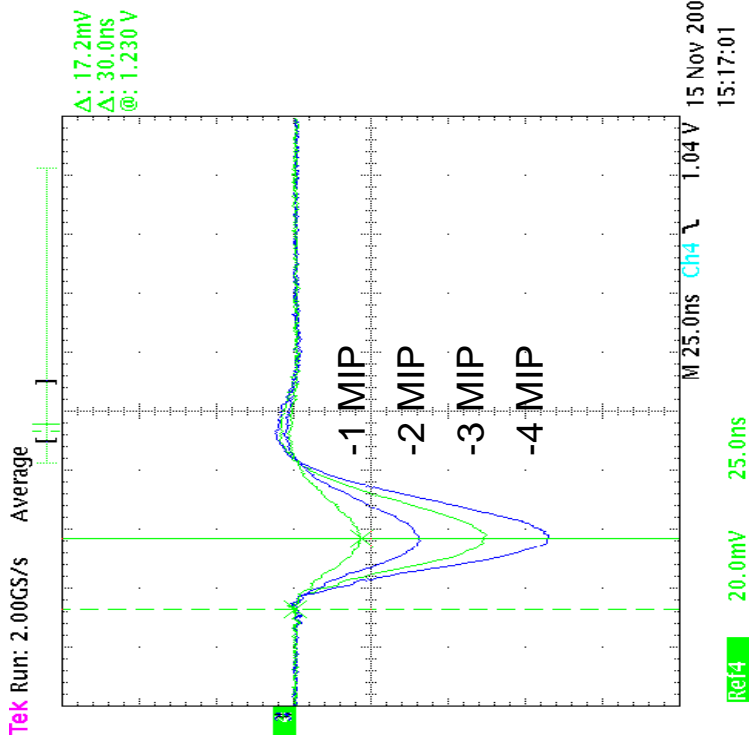
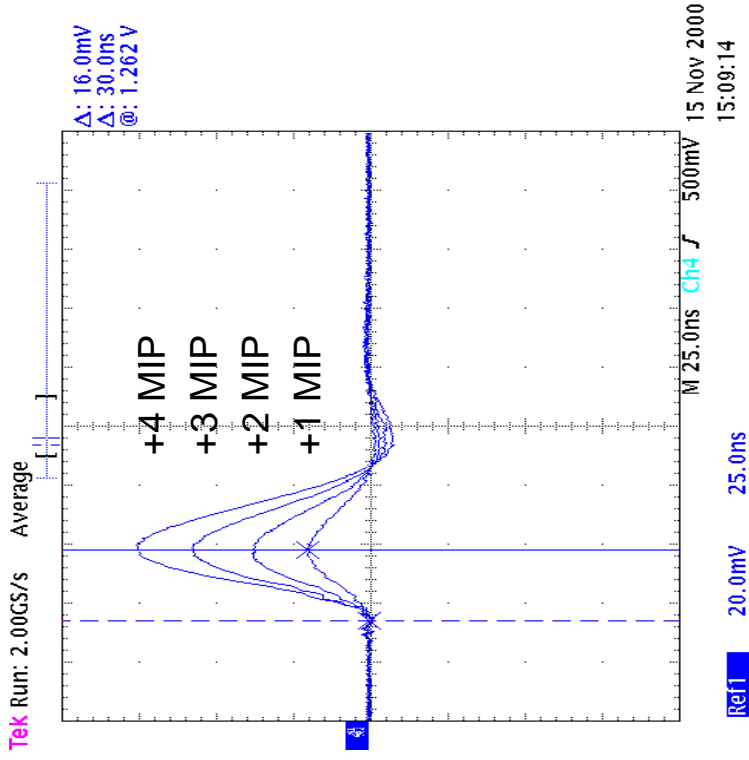


# Layout of Beetle1.0



# Frontend Amplifier

## Measurements done at Testchannel on Beetle1.0



**Risetime is too slow!**  
 measured: 30 ns  
 simulated: 19 ns  
 (on BeetleFE1.0: 22 ns)

**Gain [mV/MIP]**  
 measured: 16 (17.2)  
 simulated: 19.2 (19.1)

(Ipre=500uA, Isha=80uA, Vfp=Vfs=0V)

Change in layout of preamplifier input transistor may have introduced parasitic capacities

# Pipeline Control and Readout Logic

## Logic seems to be fully functional !

- ◆ WriteMon/TrigMon signals change their distance according to programmed latency
- ◆ Triggers are accepted and stored correctly within the logic:
  - ◇ Each trigger reduces the cycle time of WriteMon/TrigMon by one cycle
  - ◇ A Trigger on column 0 lets WriteMon/TrigMon disappear
  - ◇ Asserting 16 Triggers the FifoFull signal becomes active
- ◆ Readout:
  - ◇ DataValid is active during readout
  - ◇ Pipeline Column Number is encoded correctly in analogue header

# Outlook and Future Plans

**Beetle1.0 suffers from some bugs, but is in principle functioning !**

## Submission on 28 February 2001

- Beetle1.1
  - ◇ fix of all known bugs
  - ◇ no implementation of additional features
- BeetlePA1.1
  - ◇ further investigation of pipeamp
  - ◇ implementation of a redundancy scheme against SEU
- BeetleFE1.1
  - ◇ different preamplifier and shaper stages

**(BeetleCO1.1)**

## Preparations for TDR

- ◇ Irradiation of Beetle1.0 (digital functionality, shaping of testchannel)
- ◇ Irradiation of BeetleCO1.0 (shaping and noise)
- ◇ Attachment of BeetleCO1.0 to detector