Status of the Beetle chips

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Beetle: Outline

Beetle 1.1

- Analog readout
- Binary readout
- Pulseshape

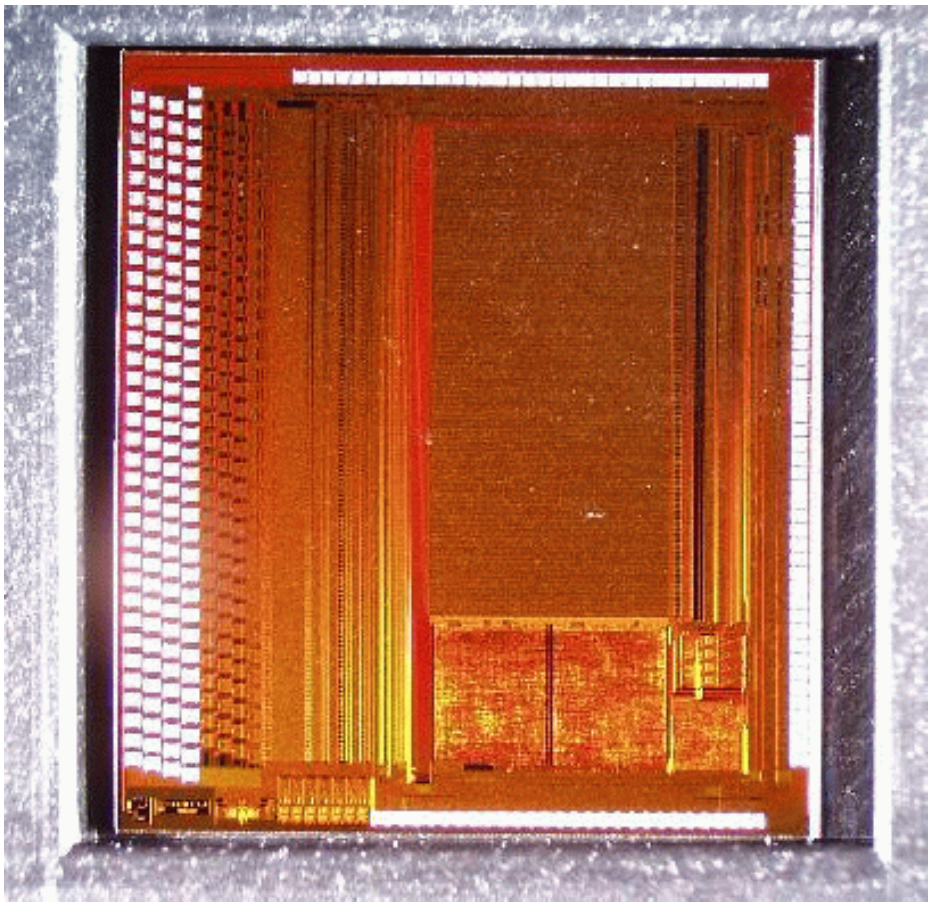
BeetleFE 1.1, BeetleFE 1.2

- Modifications
- First measurements

BeetleSR 1.0

- Schematics

Outlook



Beetle 1.1

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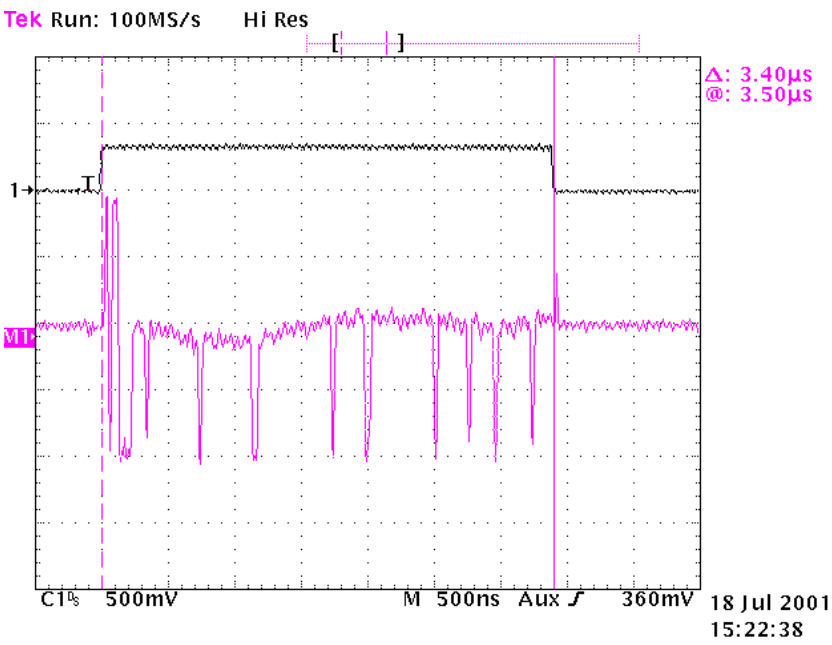
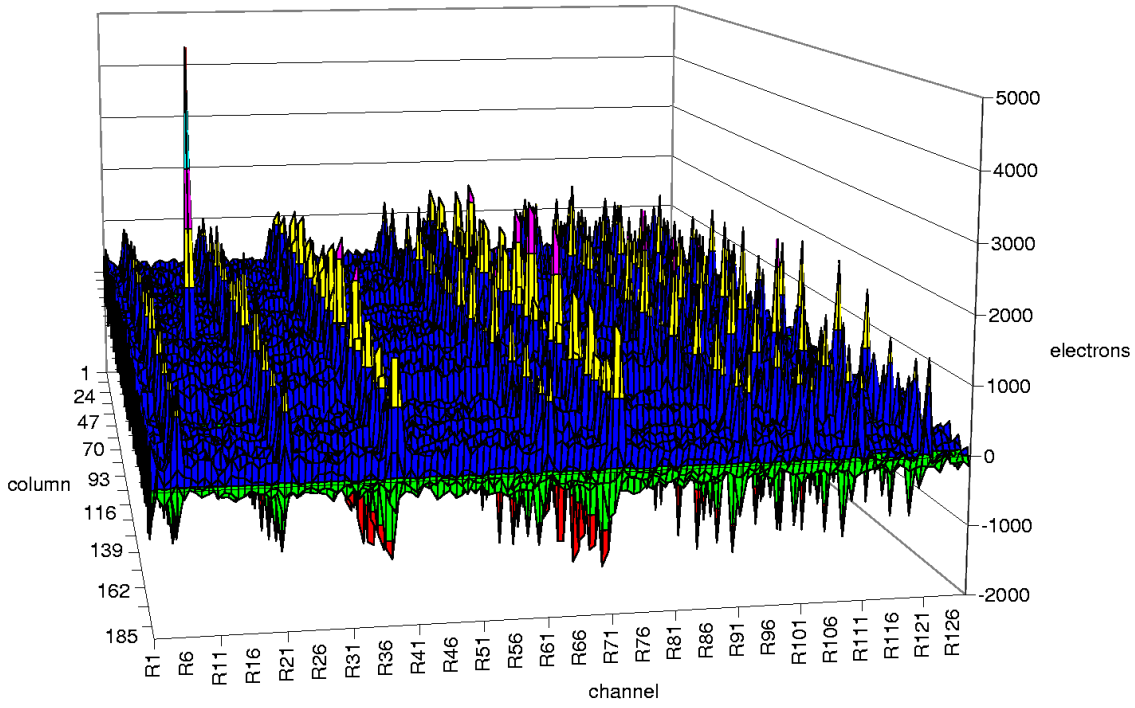
Beetle: Analog readout



128 channels on one port



Pipeline homogenity

Analogue readout shows the expected behaviour:

- flat baseline
- correct levels of encoded pipeline column number
- expected frontend gain
- pipeline homogenity better than 1.000e⁻

due to some modifications from 1.0 to 1.1

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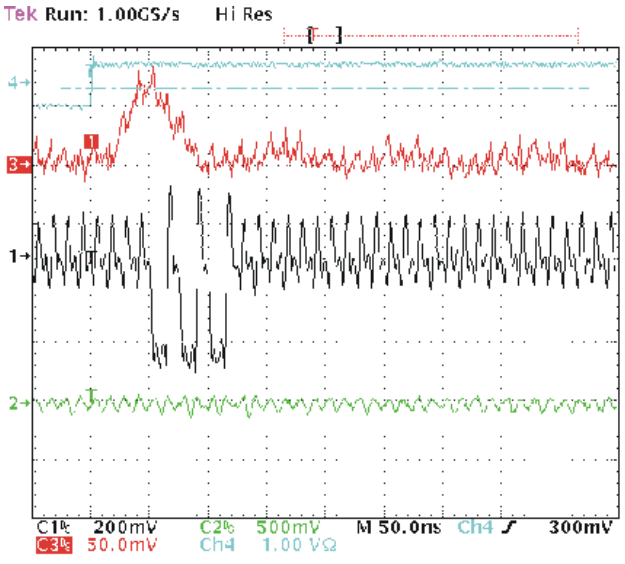
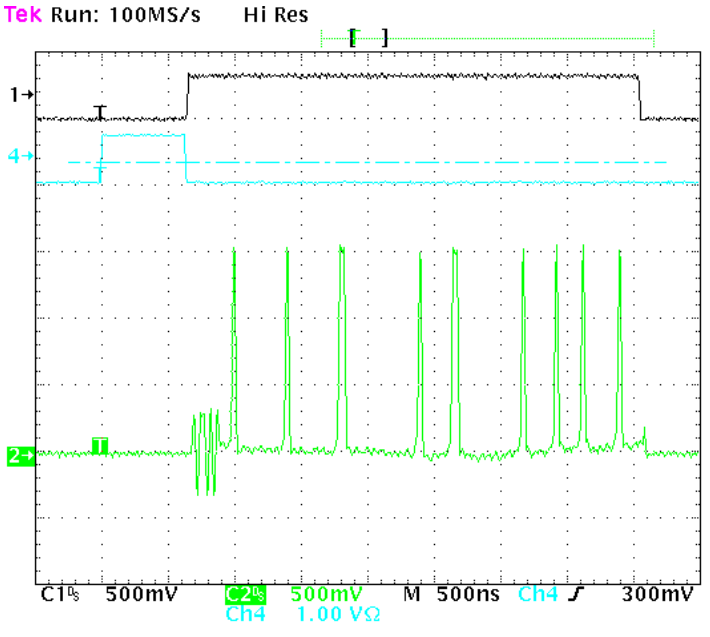
Beetle: Binary readout



Comparator in transient mode

- 80 MHz LVDS signal
- "on" as long as signal is over threshold



Comparator in peak mode

- 80 MHz LVDS signal
- "on" only for one bunch crossing
- one BX dead time to rearm comparator

Binary readout mode

- comparator signal latched into pipeline
- "on"-level = 10 MIP as designed
- PCN = +/- 2 MIP

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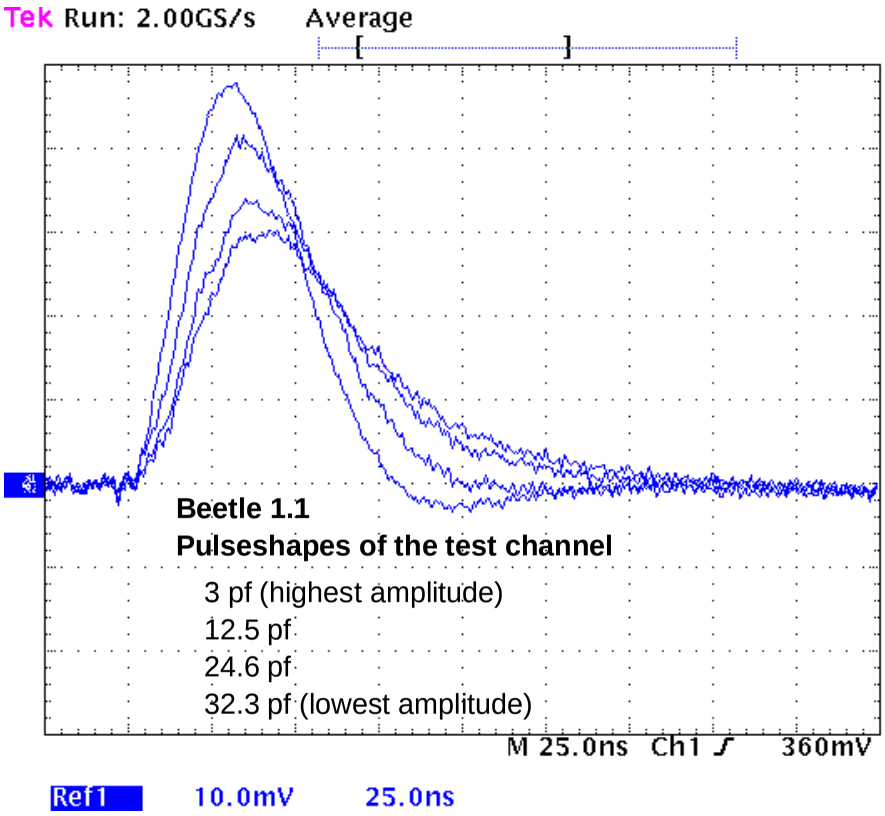
Beetle: Pulseshape



Characteristics

- peaking time 27 ns
- 30% remainder after 25 ns
- problems to keep up with LHCb specifications at higher C_p (expected especially for ITR)
- input charge rate limited to 2 nA due to feedback transistor (=0.32% strip occupancy)

→ development of new frontends

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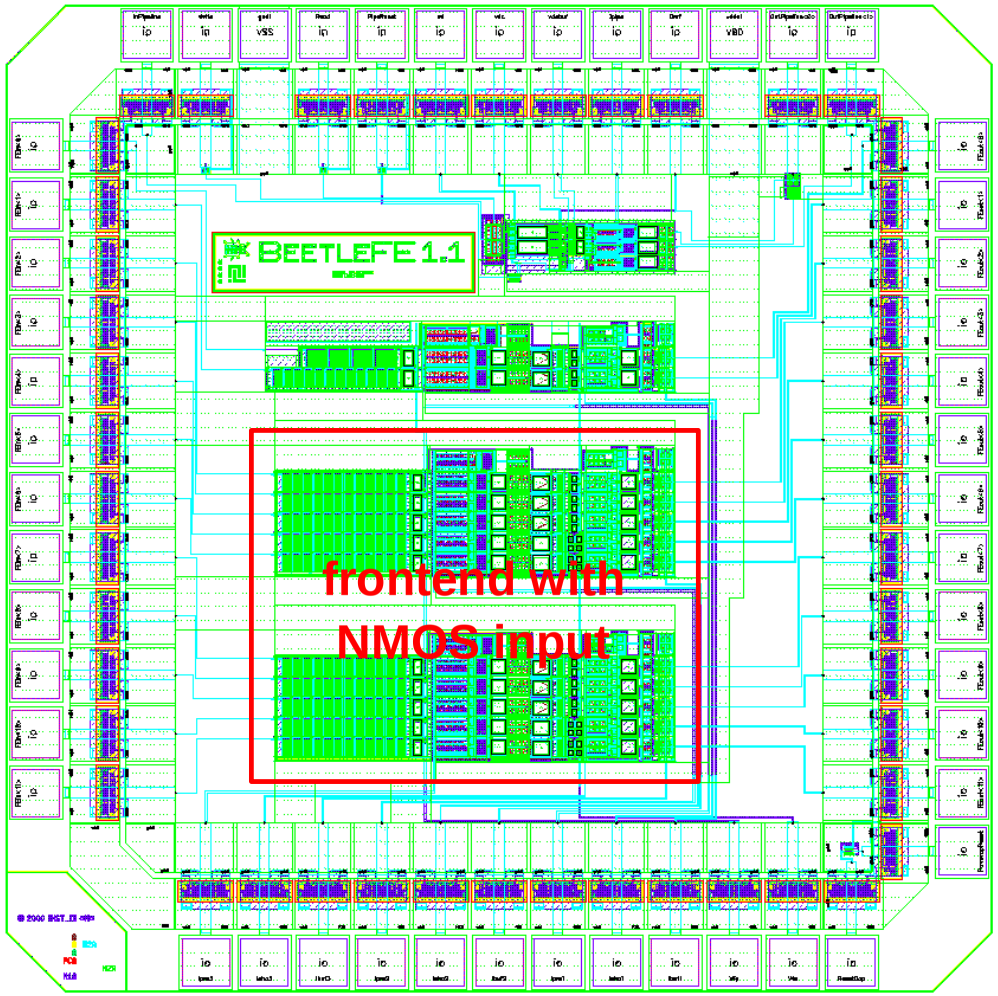
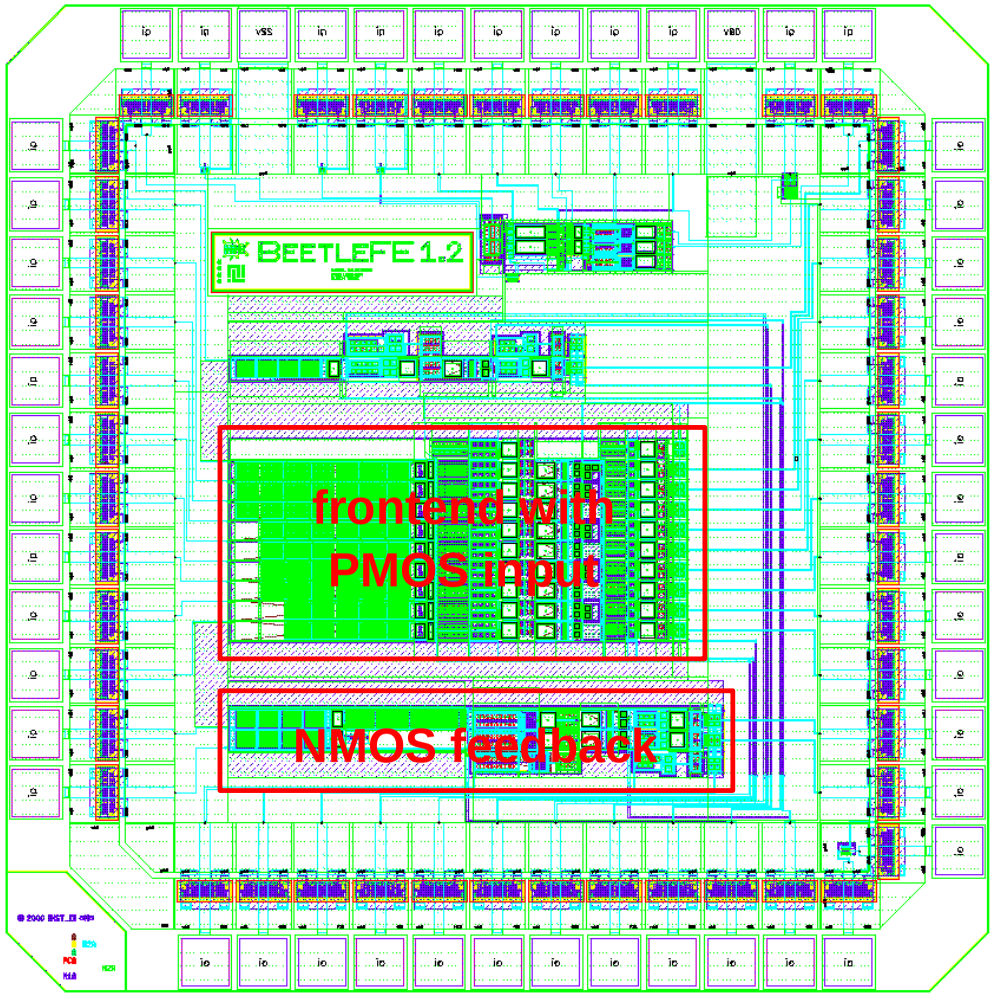
BeetleFE 1.1 & 1.2: Layout





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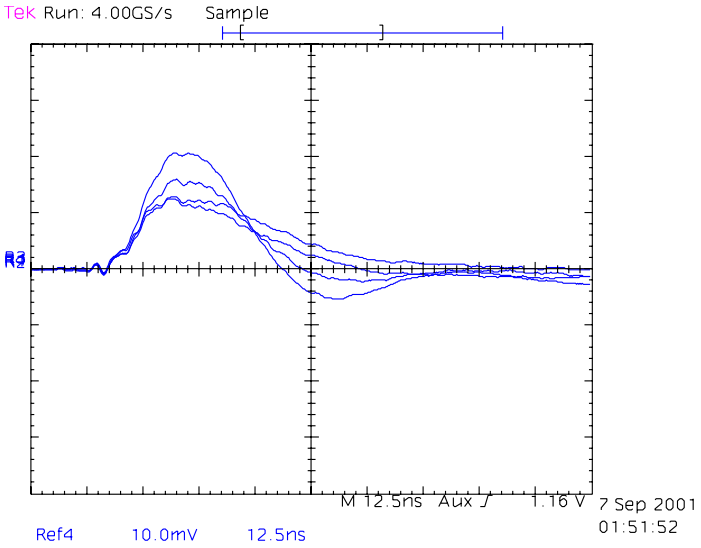
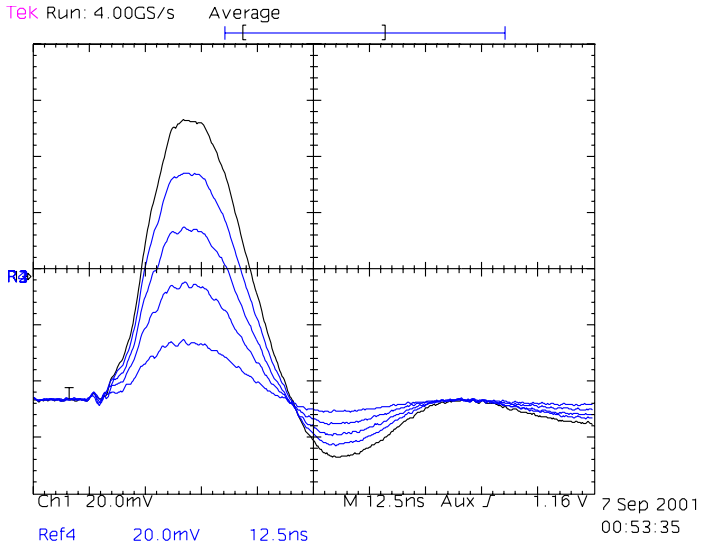
BeetleFE 1.1: First results





Different frontends

- different preamp feedbacks
- different shaper feedback capacitances

to be measured:
- **max. charge rate**
- **S/N**

Different input charges

charge	peaktime	@ 25 ns
5 MIP	19.2 ns	-8.9%
4 MIP	19.2 ns	-8.4%
3 MIP	19.2 ns	-10.7%
2 MIP	19.0 ns	-13.3%
1 MIP	18.5 ns	-21.2%

1 MIP = 11.000e$^-$ C_p = 3pF

Diff. load capacitances

C_p	peaktime	@ 25 ns
3 pF	18.5 ns	-21.2%
10 pF	21.3 ns	-21.7%
20 pF	22.9 ns	-16.5%
30 pF	24.3 ns	-16.3%
40 pF	26.9 ns	-12.9%

charge = 1 MIP

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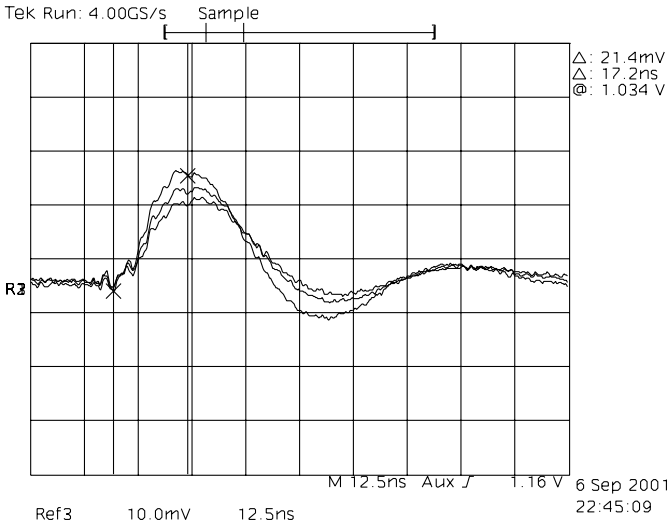
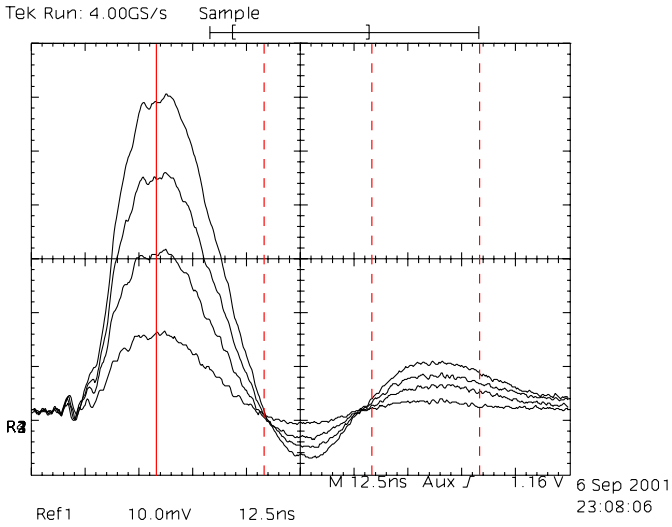
BeetleFE 1.2: First results





Different frontends

- different W of input transistor
- different shaper feedback capacitances

to be measured:

- **frontend with different load capacitances**
- **S/N**

Different input charges

charge	peaktime	@ 25 ns
4 MIP	19.7 ns	-2.9%
3 MIP	19.5 ns	-3.8%
2 MIP	19.2 ns	0.0%
1 MIP	19.0 ns	2.4%

1 MIP = 11.000e^- C_p = 3pF

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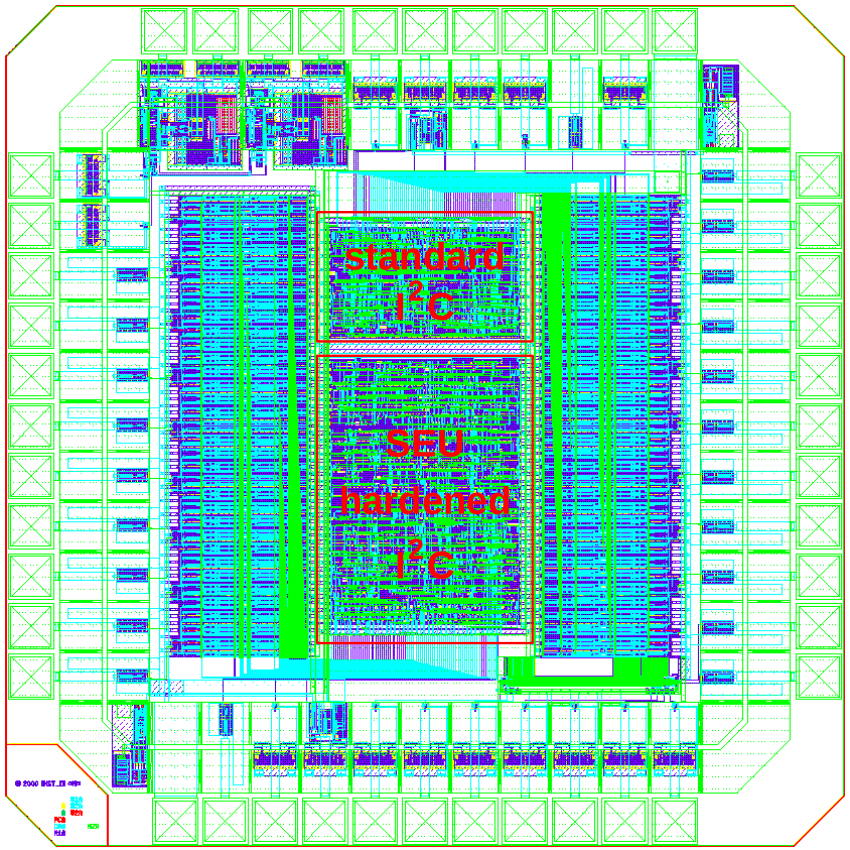
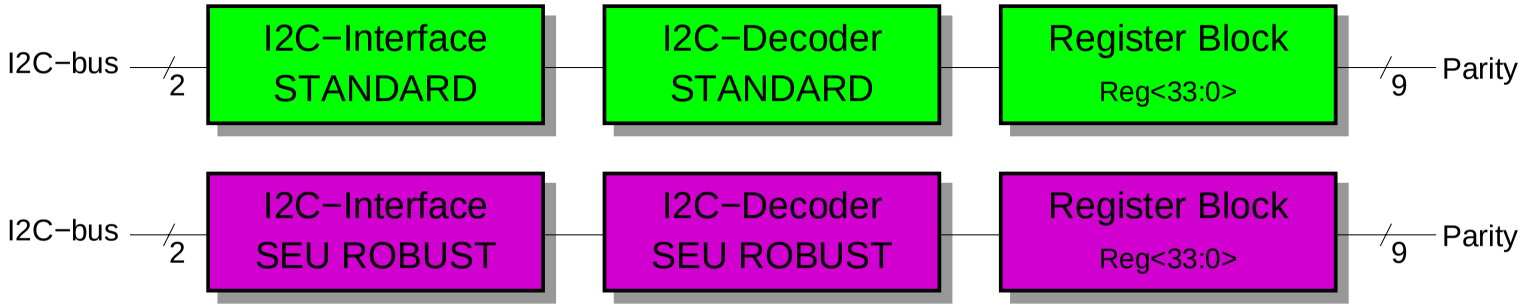
BeetleSR 1.0: Overview



BeetleSR 1.0 consists of:

- standard I²C-interface and decoder
- single event upset (SEU) hardened I²C-interface and decoder
- 2 blocks of 34 registers
- 2x9 pads indicating the parity of 32 register bits each



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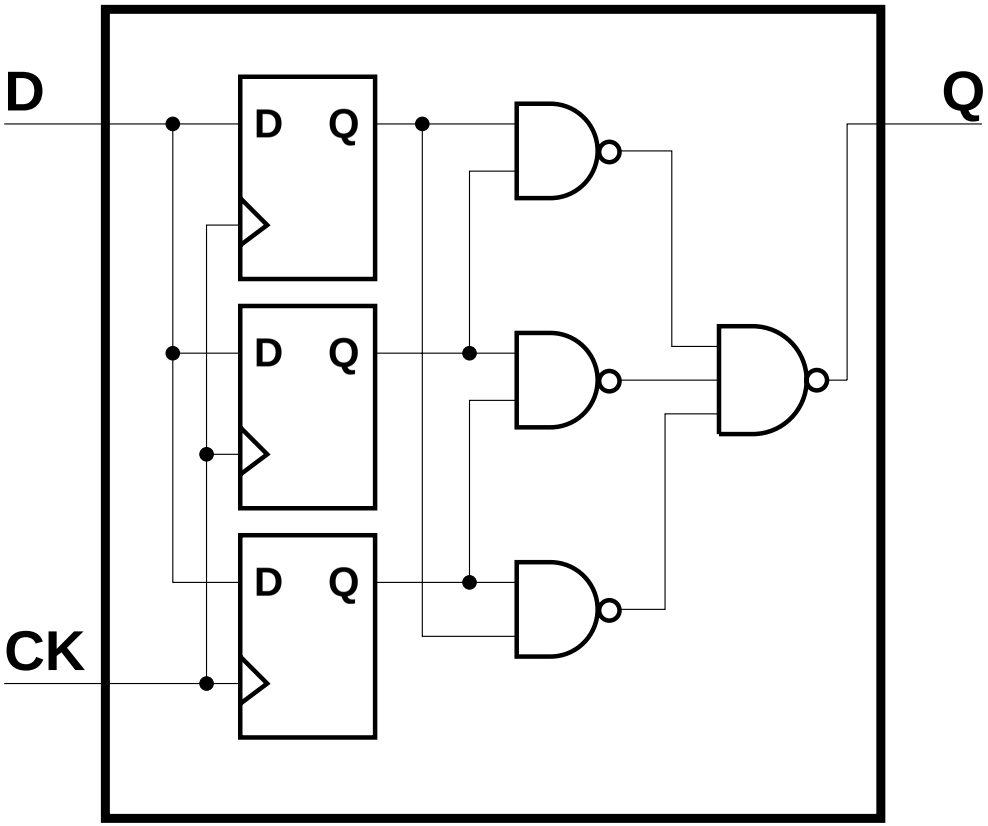
BeetleSR 1.0: Principle & planned tests

Principle of SEU-hardened logic on BeetleSR 1.0

- triple redundant flipflops
- majority decoder



Measurements with BeetleSR 1.0

- SEU rate vs. Flux from register banks
- SEU supression factor from triple redundant logic

SEU-hardened logic on Beetle 1.2

- **triple-redundant registers in switching parts of the circuit**
  - state machines
  - important registers (e.g. latency)
- **error correction with hamming codes for static circuits**
  - bias registers
  - comparator registers

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Beetle: Future plans and outlook

Beetle 1.1

- S/N measurements with new testboard
- system test with detectors is under preparation
- test for 10 Mrad radiation hardness planned for October
- test beam planned for October

Beetle 1.2

- submission scheduled for April 2002
  - one of the new frontends
  - SEU robust logic circuits
  - differential output driver with bipolar current
  - minor improvements on comparator discriminators

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