Report of the BEETLE1.2 review.

Heidelberg, 22 January.

Compiled by J. Buytaert

Introduction.

This report is a compilation of the individual reports written by Helmut Spieler (HS), Jan Kaplon (JK), Jorgen Christiansen (JC) and Jan Buytaert (JB). The original text of each contributor is kept. The various remarks and recommendations are merely grouped according to subjects. The spirit of this review was very constructive, quoting our external reviewers:

(HS) “Overall, the Beetle design team should take my comments as suggestions. I realize that other considerations come into play in the choice which course to take. Overall, the design team has done a fine job. I hope my comments are helpful”.

(JK) “I hope that my comments will not upset the VELO team and will be somehow helpful”

General remarks.

1. The chip is currently in a state that is suitable to readout the VELO detector, except for the recently uncovered problem in the output drivers (see point 34 below) that must be corrected.

2. (HS). Data from test measurements were shown without comparison with expected results from simulations. Recommend: Simulate each test setup to determine whether measured results are in agreement with design goals.

3. (JC). All problems (sticky charge, etc.) found in Beetle 1.2 must be well understood, and have been re-generated in simulations, before design changes are made.

4. (HS). Simulations were shown for nominal process parameters, but system sensitivity to parameter variations was not reported. One timing problem (related to sticky charge) was reported that can be “fixed” by using the trailing edge of the appropriate control pulse. Recommend: Perform simulations with corner parameters. Verify timing margins over full temperature range to be encountered in tests and final operation. Determine sensitivity to clock frequency and pulse duty cycle.

5. (JC). Changes to the digital part should if possible be made without making a completely new place and route. It should be done either manually or using an incremental place and route. Making a completely new P&R will give significant risks of new bugs emerging (clock skews, etc.).

Front-end.

6. (HS). Noise simulations and measurements were presented for a simple capacitive load on the preamp input. Cross coupling of noise from the neighbor channels was not evaluated. Recommend: Perform simulations with a realistic detector model, which includes inter-strip capacitance and strip resistance. Measure noise with capacitors connected to the neighbor channels in addition to capacitance to ground. Measure noise occupancy vs. threshold to determine deviation from Gaussian amplitude distribution (level of external pickup).

7. (JK). Although the noise slope shown in measurements is promising, the other parameters of the FE are not ideal. The low gain and its large dependence on the input capacitance (also variation of the peaking time) suggest insufficient bandwidth of the preamplifier causing its relatively high input impedance. The use of that chip with the input capacitance higher than 20pF is a question mark (keeping the specifying 5% cross-talk). Operating the whole chip with the FE providing only 8mV/fC is difficult in terms of excess noise from the ADB pedestal non-uniformity and switching noise. (editing note : with the new 45-degree design, the expected strip capacitances are all in the range of 6-8pf. The 15pf range was for the long strips in the 90-degree sector. However, IT and TT strips have >>20pF.

8. (HS). It was indicated that power supply rejection ratio (PSRR) is small, at best. Recommend: Simulate PSRR vs. frequency and confirm with measurements. This is always a weak point, but simple changes can sometimes make a big difference (e.g. connection points of bypass capacitors).

9. (JC). Power supply rejection should be simulated and measured.

10. (JB) The pedestal baseline of beetle1.2 shows a sagging trend. This is assumed to be a consequence of the asymmetric (top/bottom) input pads for analogue vdd and gnd. A new Beetle (version for MAPPMT), with symmetrical distribution of these pads, is currently in fabrication. Depending on the result, this will be implemented on version 1.3. The reviewers recommend strongly that it is in general a good practice to provide power to the front-end symmetrically from both sides of the chip.

11. (JB) The quoted noise formula 450 + 45 e/pF is measured just after the front-end amplifier only. It therefore does not yet include contribution from pedestal non-uniformity of the pipeline cells.

Comparator.

Lack of clear electronic specifications:

12. (HS). Several parameters appear to be marginal, e.g. noise at detector capacitance >20 pF, dispersion of comparator thresholds, response time of input stage and others. The input noise and the dispersion of the comparator threshold affect the minimum detection threshold and inadequate gain-bandwidth product in the preamp can lead to excessive cross talk to neighboring channels. Recommend: Prepare a requirements document that links physics requirements to electronic design specifications.

13. (JK). No electronic requirements exists for this stage. Suggestion: make the specification for that stage including the operating threshold (1fC?), the minimum detectable signal (1.2fC?), and the maximum detectable signal (10fC?) and specify the maximum time walk of the chain FE/comparator (16ns?). The results of such a simulation can be a basis for the review of that stage.

14. (JC). "Physics" requirements (threshold, resolution, time walk, etc.) to the comparators must be defined.

Too large channel-spread of offset (= '0-threshold' level), compared to MIP signal.

15. (JK). The low gain in the front-end sets very tough requirements for the performance of the comparator, which will has to work probably with the overdrives below 1mV (the matching calculated in MIP also depends on the FE gain but it might be corrected with the DAC).

16. (HS). Comparator threshold dispersion is excessive. A proposed change to extend the range of the trim-DAC to 5 bits was presented. It is not clear what the required threshold level is to obtain an acceptable combination of efficiency vs. noise occupancy. (This should be addressed in the requirements document.) Recommend: Investigate possibilities to increase signal gain before the comparator. One possibility is to optimize the source followers preceding the comparator. Another is to increase the gain-bandwidth product of the preamp. From the presented circuit diagrams it appears that the high-impedance node of the preamp is connected directly to the shaper input. This probably increases the capacitive load beyond what could be achieved if a buffer stage with minimum input capacitance were introduced. Increased gain-bandwidth product would allow a higher charge sensitivity dVout/dQin and also allow a lower input impedance to reduce cross talk. Of course, these are opposing goals, but

increasing the gain-bandwidth product provides more latitude in establishing an acceptable compromise.

17. (JC). It must be clearly defined for the users that read back (and re-write) of the threshold registers and test-pulse channel-mask cannot be done while the chip (comparators) is in actual use.

18. (JC). Quite significant changes to the comparator circuits are proposed. It should be insured that malfunction of the new comparator block will not prevent the normal analog readout to work.

19. (JC). The proposed DAC architecture for the local threshold adjustment must be carefully evaluated for radiation effects

Pipeline memory.

20. (JC). Beetle 1.2 pedestal variations over analog memory must be presented and their effect on noise (when not having memory location compensation) must be calculated. Automated test procedures should exist to allow fast characterization of new versions of the beetle (e.g. memory pedestal maps). It should not take 6 months to get a new version characterized with manual test setups.

21. (JB). The memory capacitor uses the gate capacitance of a standard NMOS. Similar designs use a ‘special device’ (also gate-thin-oxide on N-well) with less dependence of cap-value on gate voltage.

Radiation hardness of the DAC’s.

22. (HS). DAC topology is more sensitive to radiation than other circuits. Effect of radiation depends on whether gate voltage is high or low. DAC outputs cannot be tested directly. Recommend: The preferred solution is to use a “radiation-hard” architecture (see ATLAS ABCD, for example). In any case, perform radiation tests with all bits set high and also with all bits set low. Check for sensitivity to dose rate. Test for possible non-monotonic response. Add test pads to allow direct measurement of DAC output levels (useful for diagnostics and wafer probing).

23. (JK). The presented DAC’s have not radiation-tolerant architecture (switching the gate voltages instead switching the currents). The safest solution, which does not require the characterization of the DAC’s with the radiation, is go to the "standard" radiation-hard architecture. For the final review it would be good if you can present also the results from the beam test analysis of the longer strips (10-16pF). The very good

numbers (S/N ~20) from the beam test are for the short strips (6pF) - correct me if I am wrong.

24. (JC). DAC's: The chosen DAC architecture may be quite sensitive to radiation effects as the matched transistors will have biasing conditions depending on programmed DAC values. This should be tested.

25. (JB) Voltage DAC's are referred to VDD, exposing bias voltages to supply noise. This is maybe only second-order to the very weak PSRR in the front-end amplifier. It is recommended to simulate and measure both.

Test-pulse.

26. (HS). Level of calibration pulse is not fully adjustable. Recommend: Based on >18 years of experience with ICs using comparators for on-chip zero suppression and binary readouts, I strongly recommend implementing a calibration system that allows threshold scans to measure gain channel by channel and extract threshold dispersion and noise levels. This is extremely useful for chip testing at the wafer-probe level, characterization of hybrids and full detector modules during assembly and monitoring of system performance during operation. Even without calibrating the on-chip test capacitors, one can expect absolute charge calibration to the 10% level. In the Beetle IC it appears to me that controlling the timing of the test pulse is not very critical, so implementing an on-chip test/calibration capability would involve only the addition of a DAC to set the test pulse level.

27. (JK). I suggest to have a possibility to inject a calibration signal to the chips mounted one the detector modules in the final system. It is necessary for the debugging of the analog system and adjusting the biases for the chips, which might drift during irradiation (since you can recover the pulse shape from the consecutive samples the variable delay of CAL signal is probably not very important). It is crucial for the binary system (also including the possibility of delaying of the calibration pulse relative to the clock phase).

28. (JB). The feature of the +2, +1, -2, -2 modulation of the test-pulse is present for historic reasons. It is now useless, given the programmable channel mask. Removing it on the other hand bears a risk of possible problems. The recommendation is to leave it in.

29. (JC). It is highly recommended that all systems incorporate ways to use the test pulse injection feature of the chip. As the Beetle does not

have a programmable test pulse delay this function must be made elsewhere.

SEU

30. (HS). Results on SEU rate were presented without relating them to the anticipated particle flux in the experiment. Recommend: Estimate SEU rate in experiment.

31. (JC). System effects from the fact that the threshold registers do not have triple redundant protection against SEU should be estimated (pile-up veto).

Reported bugs.

Sticky charge.

32. (HS). A plausible explanation for the “sticky charge” phenomenon was presented, but without simulations to support it. Recommend: Full simulation of original circuit and proposed circuit changes to confirm origin of “sticky charge” effect and its cure. Compare with other pipeline designs that do not show this problem.

33. (JC). Proposed change for sticky charge problem means using the falling edge of clock. A clear specification of clock duty cycle must be made and this must be verified to be compatible with systems.

Gain drop @ 2.6V.

34. (HS). Permanent gain degradation was observed when the supply voltage was increased beyond 2.6 V (0.1 V beyond nominal supply voltage). Recommend: Find problem – this is serious. Establish required supply voltage range over which IC is to operate while meeting specifications. Determine maximum supply voltage variations in final experiment (e.g. due to cabling resistances), also when one or more ICs should fail.

35. (JK). Problem of the output buffer (permanent gain degradation at Vcc >= 2.6Volt) should be debugged and possibly corrected.

36. (JC). Problem of destructive failure of output driver at increased power supply voltage must be understood and corrected.

Beetle 1.3

Risk.

37. (JC). Many small changes are proposed. Each of these may not look significant but the total number of changes will give a certain risk that the next submission could fail.

Planning.

38. (JC). Each user should determine the planning effects of the need of an additional prototype submission (delay of ~6 months). The current planning with a MPW submission in May-June 2003 and the final engineering run submission in August-September 2003 seems far too optimistic. More time should be allowed to characterize the new version before making the engineering run.

39. (JC). It is recommended to have a specific design review with a few external chip designers before the Beetle 1.3 submission.

40. (JC). It must (if possible) be insured that Beetle 1.3 have a chip size and pad layout compatible with hybrids being designed for Beetle 1.2. (Related to proposed changes of power pads and possible increase of chip size with change of comparator design).