ASIC-Labor Heidelberg

Beetle 1.0 - A new Readout Chip for LHCb

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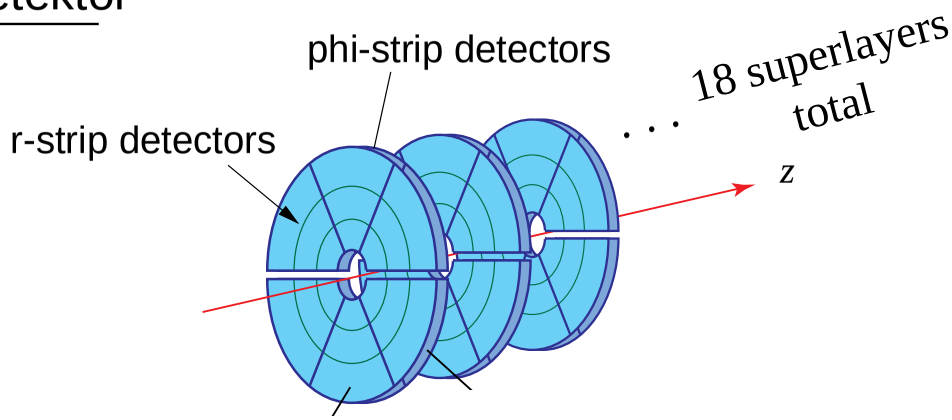
Overview

- Specifications from LHCb
- Architecture of the Beetle 1.0
- Analog stages (simulation and measurements)
- Methods to enhance radiation tolerance
- Layout of the readout chip
- conclusions future plans

Goal: Readout Chip for the LHCb Vertex Detektor

- Silicon microstrip detectors (150um)
- 1MIP=11.000 electrons
- 10pF strip capacitance
- single strip occupancy ~3%
- 220.000 channels
- readout pitch: 40 - 60 um



→ pipelined analog readout for tracking part of detector
→ derive immediate trigger signal for pileup-veto

- Radiation Dose: up to 2MRad/year => 10MRad total dose

Use of the same readout chip in other subdetectors:

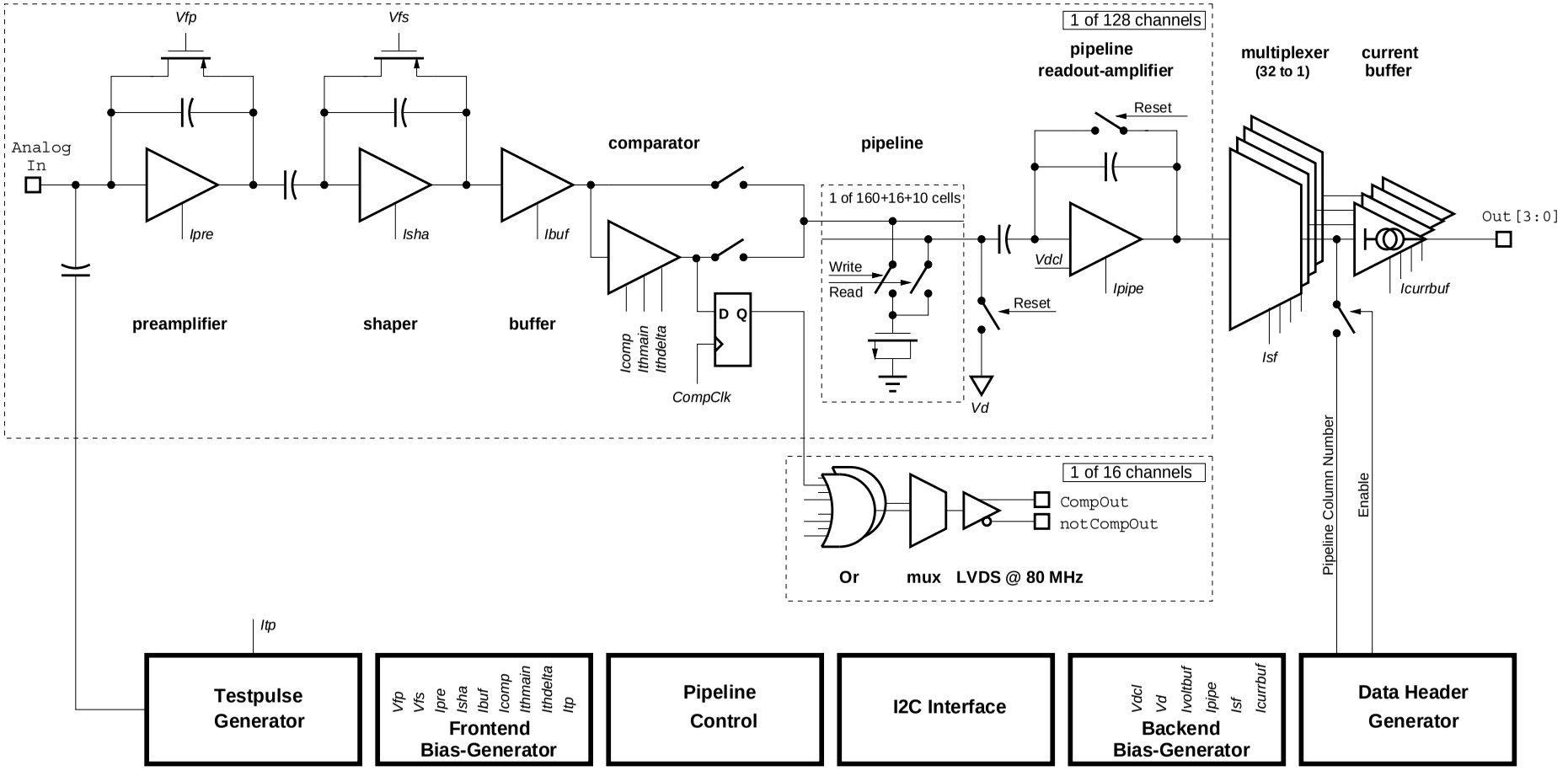
- Inner tracker (microstrip gaseous chambers or/and silicon strip detectors)
- RICH backup technology solution (multi anode photo multiplier tubes)

Key Parameters of Readout Chip:

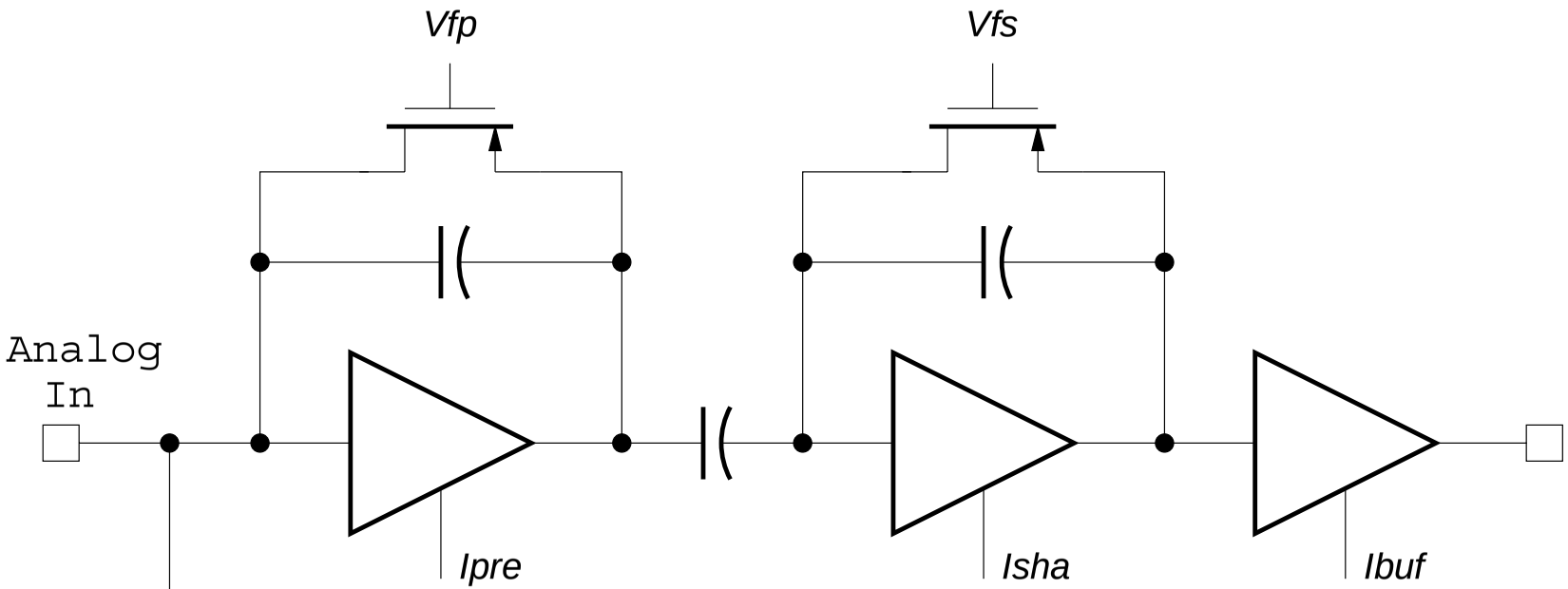
- Sampling frequency: 40 MHz
- L0 trigger rate: 1MHz
- Readout time per event: 900ns
- Latency (160x25ns) = 4us
- Number of multievent buffer: 16
- deadtimeless readout

- max. power consumption: < 4mW/channel
- S/N required by vertex detector: >14
- total accumulated dose: 10 MRad

Block Diagramm of the Beetle 1.0



Frontend Amplifier:



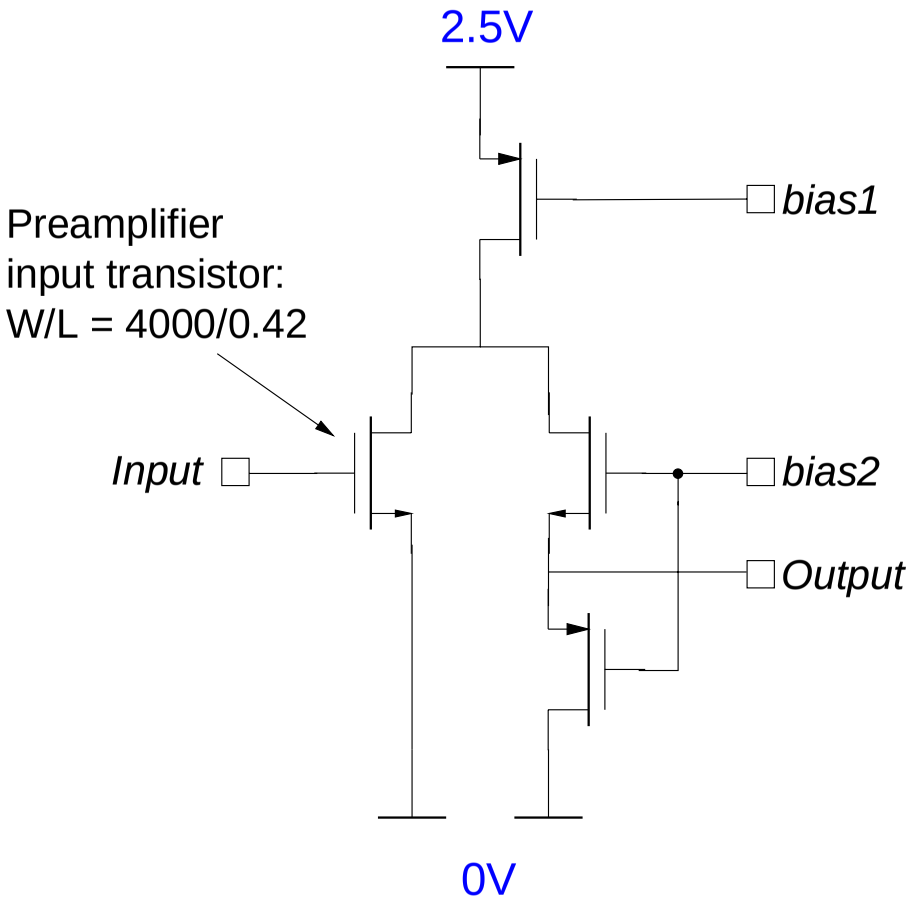
charge sensitive preamplifier

active RC-CR shaper

source follower

Testpulse injector

Core Cell of Preamplifier / Shaper: Folded Cascode Configuration

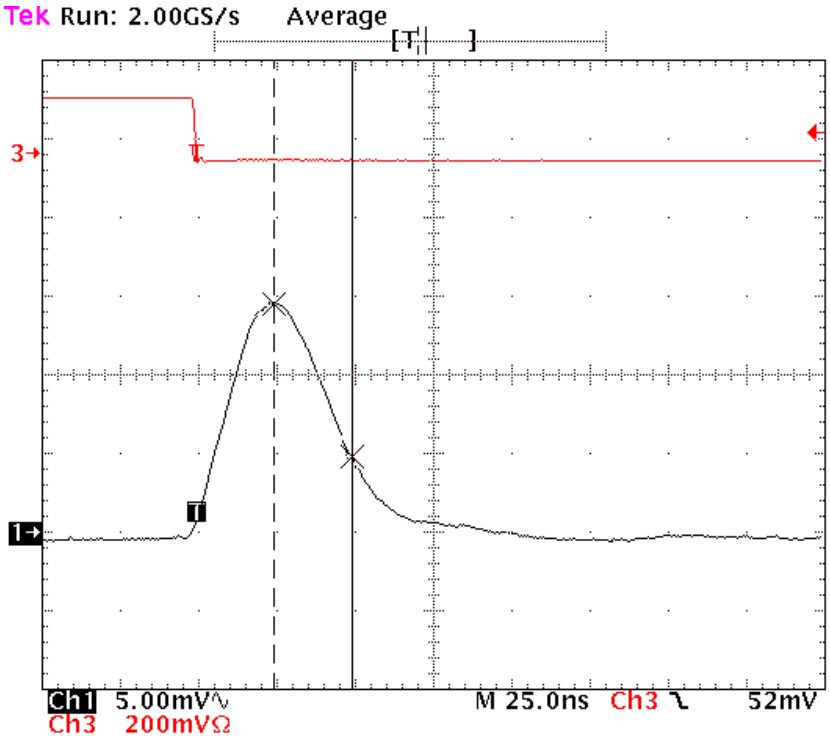


Measured noise of Frontend with testchip:

ENC = 303e + 33.6 e/pF
at Ipreamp = 600uA

total power consumption of frontend: 1.88mW / channel

Measurement with testchip



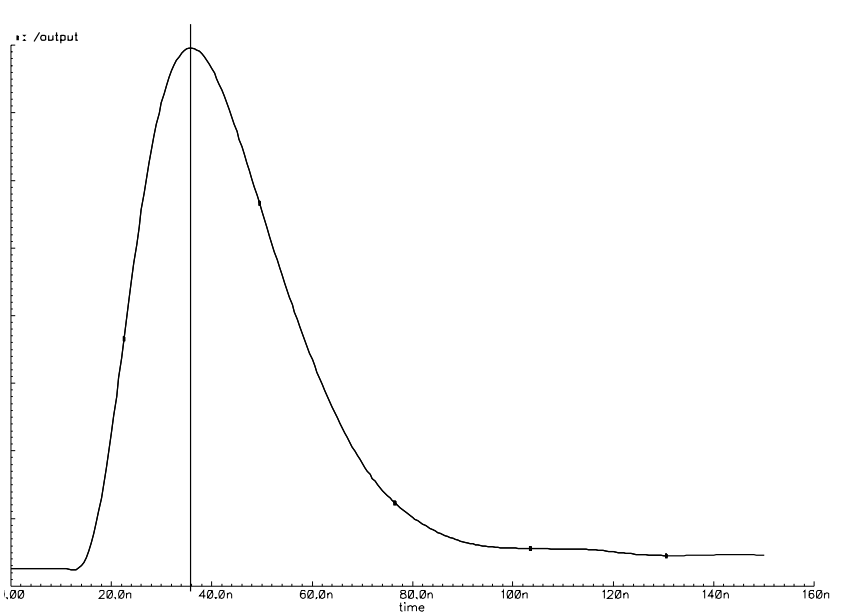
risetime = 25ns

gain = 14.5 mV / 11.000e

remainder after 25ns = 30%

Simulation of input stage

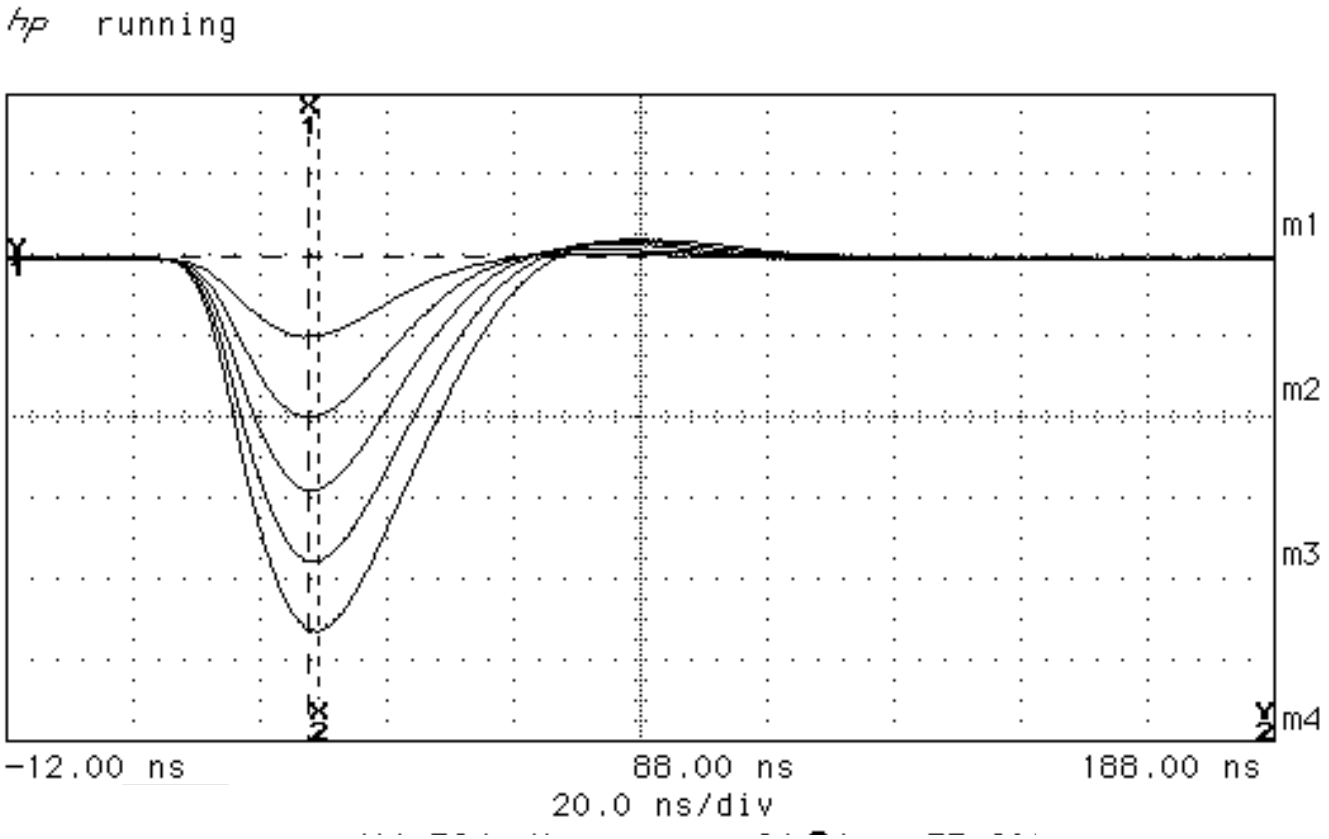
Transient Response 1MIP @ Cload=10pF



risetime = 23ns

gain = 14.5 mV / 11.000e

remainder after 25ns = 25%

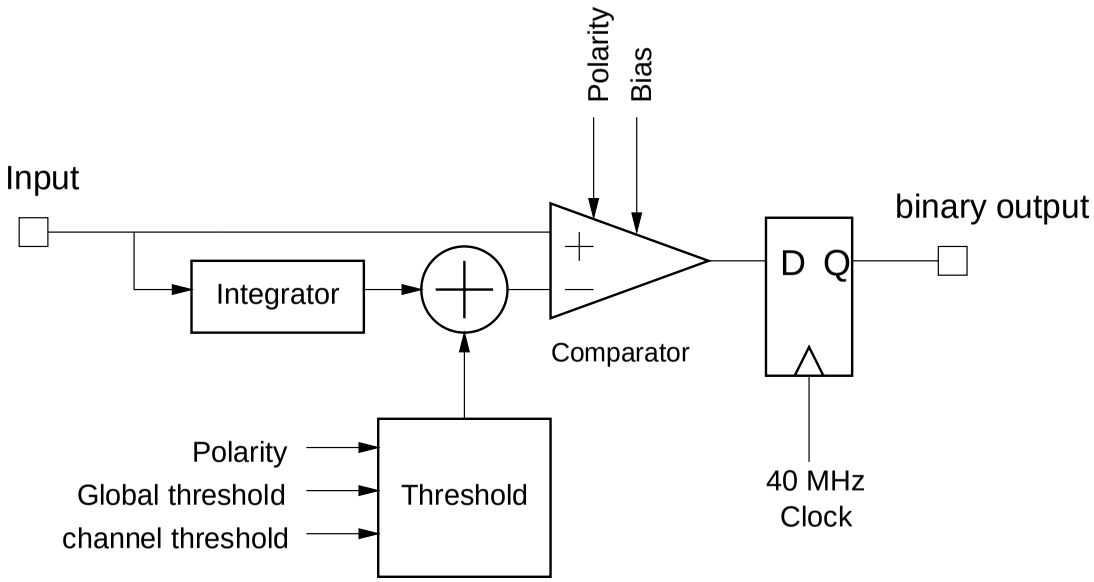


Dynamic range:
+- 10 MIP
(= +- 110.000e)

at power consumption
of 1.88 mW / channel

peak time does not
shift for higher signals

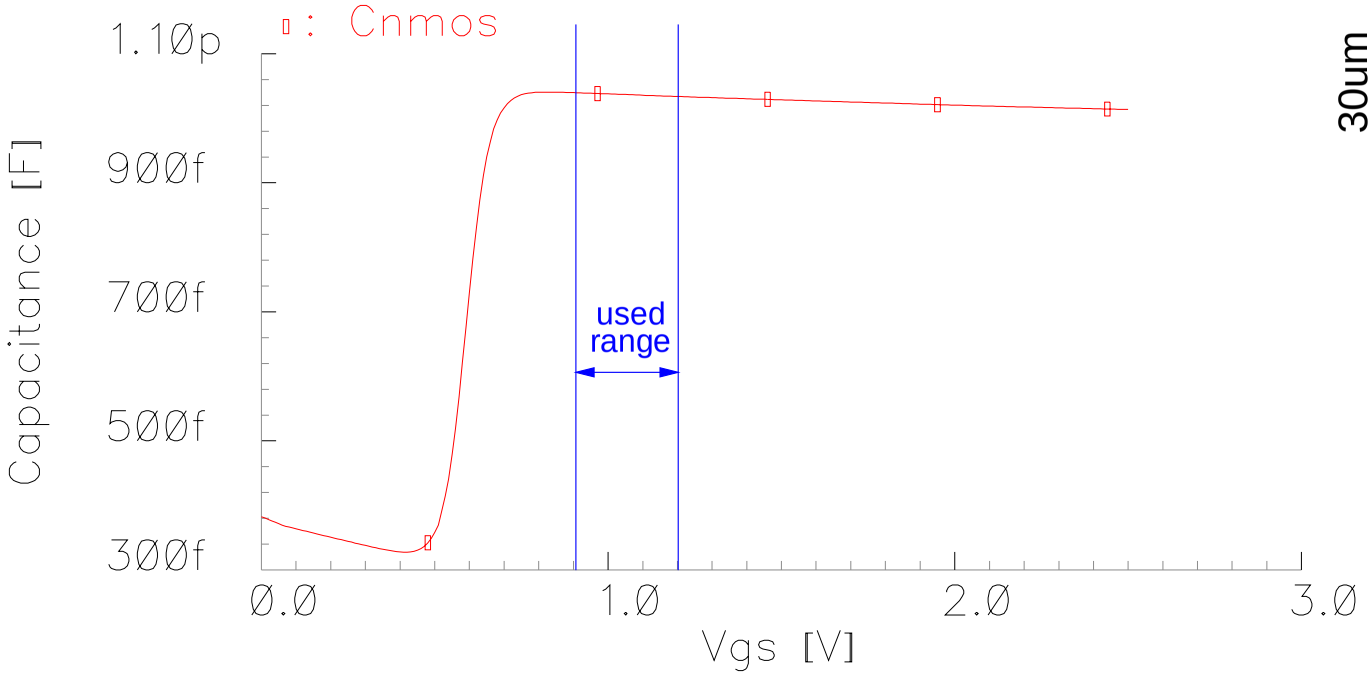
Comparator:

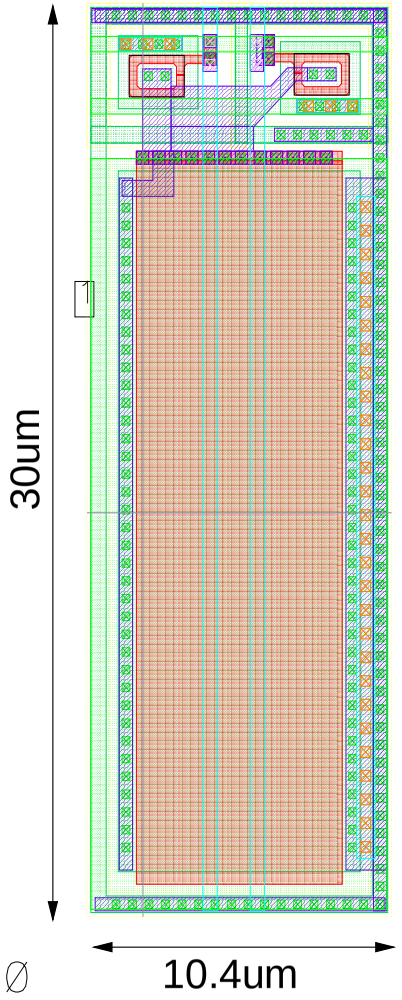


- adjustable threshold for each channel
- binary output:
  - -> either stored in pipeline
  - -> or imediately brought off chip
- time constant of integrator: 5us

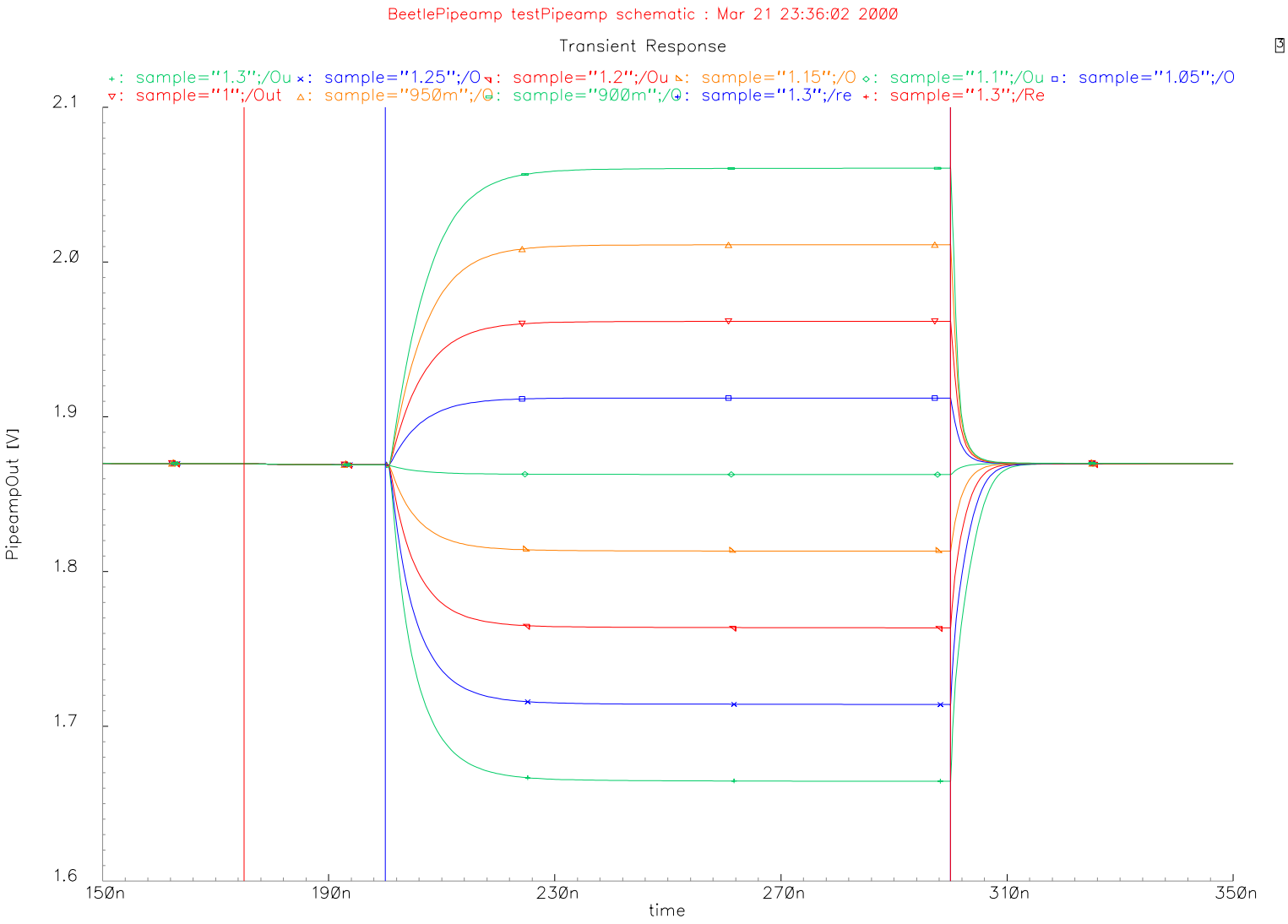
Analoge Pipeline:

- 129 x 186 n-mos gate capacitors
- 2 enclosed n-mos as read/write switch
- Capacitance 1pF





Pipeline Readout Amplifier:

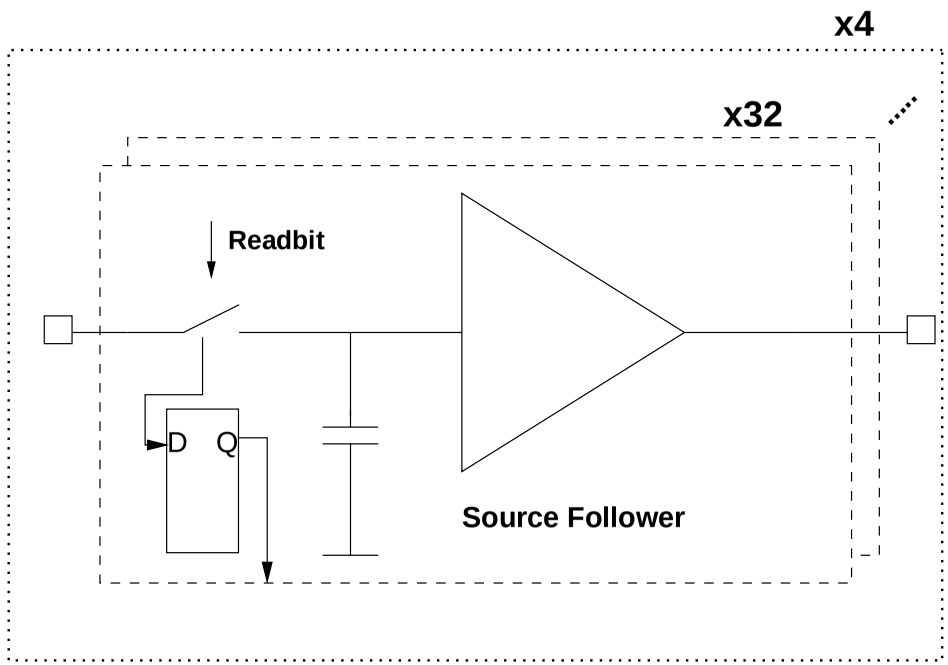


- Resetable charge sensitive amplifier
- Rise time well below 75ns

- folded cascode configuration used as opamp cell

Multiplexer:

- Sample/Hold stage with source follower
- different multiplexing modes by switching of "Readbit"



1.) 32 channels to 1 output port

x4

for analog readout at 40MHz
=>900ns readout time per event

2.) 64 channels to 1 output port:

x2

for binary readout at 80MHz
=>900ns readout time per event

3.) 128 channels to 1 output port
for analog readout at 40MHz
=> slow readout for test setups etc.

Bias Blocks:

- 10bit voltage DACs
  using R2R resistor ladder
- 10 bit current DACs

- reference current using:
  cascoded transistors with
  20k reference resistor
  -> current sources on 20 tested prototype chips
  show spread of < 5%

Pipeline and Readout Control logic:

- identical to control logic in HELIX128 readout chip
- functional description in Verilog
- Synthesis with Synopsys
- Place and Route using 3 metal layers with Silicon Ensemble
- Size: 1.9mm x 0.8mm

Slow Control of Readout Chip:

I2C-Interface:

Assignment of chip address in a self-programming procedure on powerup

38 Register write/read

- bias settings for amplifier
- latency
- readout mode
- readout clock frequency programmable

future: parity register

mask register for testpulse, comparator

fail safe token for address generation

different Resets possible (controlled by length of external reset):

-softreset: resets contents of multievent buffer
-hardreset: resets trigger & write pointer
-powerupreset: resets all register contents

Design techniques to enhance radiation resistance:

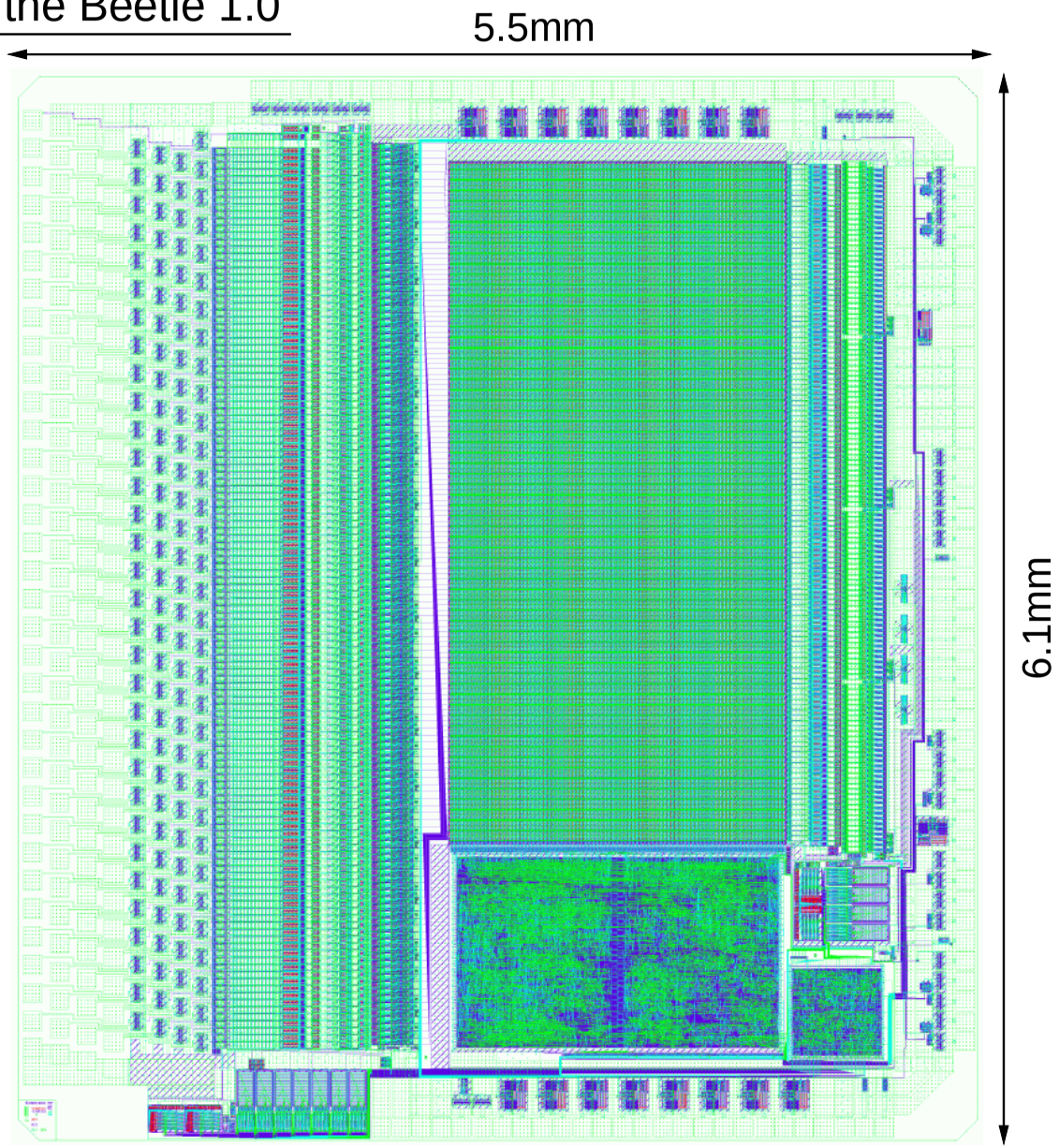
- minimize threshold voltage shift by choice of technology
- edgeless n-mos transistor layout to reduce leakage current
- systematic use of guardrings to minimize SEE rate

(Total Dose and Single Event Effects (SEE) in a 0.25um CMOS Technology, F.Faccio et al. in CERN/LHCC/98-36)

- forced bias currents / node voltages not fixed
- passive components used as negative feedback

(e.g. RD20 or HELIX128, W. Fallot-Burghardt et al. in HD-ASIC-33-0697)

Layout of the Beetle 1.0



input
pitch:
41um

->50um
overall

Summary:

- Based on good experience with 2 testchips, we expect to have a readout chip, which fullfills the LHCb requirements
- If basic funtionality is given:
  -> characterization in lab
  -> test with detector as soon as possible
  -> irradiation as soon as possible

Submission of Beetle 1.1 planned for end 2000 / start 2001

additional features:

- JTAG protocol to enable boundary scan
- parity check of all registers to enable SEU detection
- introduction of mask register for testpulse and comparator
- modification of output current buffer

Find further status reports on:

http://wwwasic.kip.uni-heidelberg.de/lhcb