
# Beetle Overview

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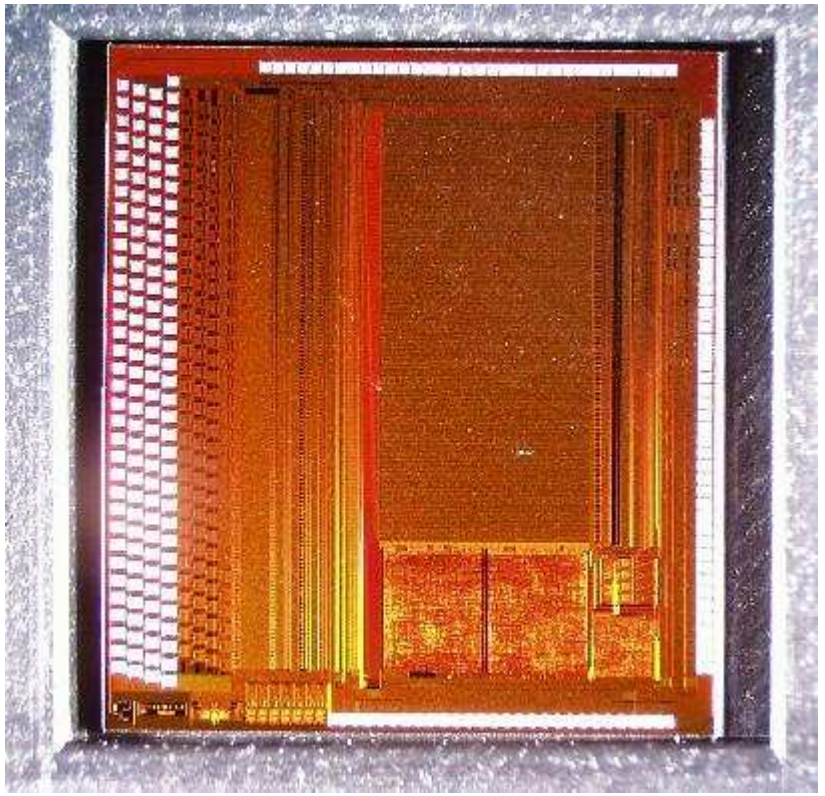
# Beetle: Outline

- Beetle Specifications
- Beetle 1.1
  - Analogue readout
  - Front end
  - Comparator
  - Pipeline / Multiplexer
  - Control Logic
- BeetleFE 1.1
  - Pulseshape
  - ENC
- Results from TID irradiation test
- Major modifications towards Beetle 1.2
- Next steps / outlook





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# Beetle: A Readout Chip for LHCb

- analog / binary pipeline chip
- providing a prompt binary readout for trigger applications
- integrated in a standard 0.25 µm CMOS technology
- designed for:
  - Silicon Vertex Detector
  - Pile-up Veto Trigger
  - Inner Tracker
  - RICH (in case of MAPMTs)

## Key Specifications:

- 40 MHz sampling
- max. latency 4 µs
- 40/80 MHz readout
- fast shaping:
  - $t_{rise} \leq 25$ ns
  - remainder 25 ns after peak $\leq 30\%$
- accept up to 16 consecutive triggers
- readout time $\leq 900$ ns / trigger
- radiation hard $\geq 10$ Mrad



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# Beetle Specification: L1 Interface

**Rather well defined**: *http://lhcb-elec.web.cern.ch/lhcb-elec/html/key_parameters.htm*

- Bunch crossing rate: 40.08 MHz
- Maximum L0 rate: 1.1 MHz
- L0 latency: 4.0 µs = 160 clock periods
- L0 gap: None
- Consecutive L0 triggers: max. 16
- L0 trigger types: only one (normal trigger)
- Samples to extract per L0 accept: one per channel (multiple samples if required)
- L0 derandomizer depth: 16 events
- L0 derandomizer readout time: (32 + 2 + 2) * 25 ns = 900 ns
- L0 restrictions: emulation of front-end buffers ⇒ predictable release of derandomizer buffers
- Bunch crossing clock and L0 distribution: TTC system
- Synchronization checks: all event data must carry synchronization checking data ⇒ PCN
- Location and qualification of L0 front-end electronics
  - 0.25 µm CMOS technology & special design rules ensure radiation hardness > 10 Mrad
- L1 buffer input speed: 900 ns minimum spacing between events
- L0 front-end reset



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# Specification: Detector Interface

| | Pile-up Veto | VELO | Inner Tracker |
|---|---|---|---|
| Readout pitch | flexible, 40-60 µm | flexible, 40-60 µm | |
| Signal polarity | positive and negative | positive and negative | |
| Pulse distribution | Landau | Landau | Landau |
| Mean signal | 11.000 $e^-$/MIP | 11.000 $e^-$/MIP | 11.000 $e^-$/MIP |
| Detector capacitance | 10 pF | 10 pF | 30 pF |
| Required S/N | | > 14, independent from irrad. | |
| Coupling to detector | AC | AC | AC |
| Single channel leakage current | 0 (AC coupling) | 0 (AC coupling) | 0 (AC coupling) |
| Radiation dose | > 2 Mrad/year | > 2 Mrad/year | |
| Chip should stand large signals | up to 400 Mips | up to 400 Mips | |
| Distance to next DAQ stage | 10 m | 10 m | 10 m |
| Required linearity | | ≤ 5% (≤ 10 MIP) | |
| Signal time jitter | | < 5 ns | < 5 ns |
| Maximum power consumption | | < 6 mW / channel | |
| Signal peaking time | ≤ 25 ns | ≤ 25 ns | ≤ 25 ns |
| Fall time, pulse spill over | < 30% after 25 ns | < 30% after 25 ns | < 30% after 25 ns |
| Analogue pipeline length | - | 160 (4 µs) | 160 (4 µs) |
| Readout time | 25 ns | 900 ns | 900 ns |
| De-randomizing buffer | - | 16 triggers | 16 triggers |



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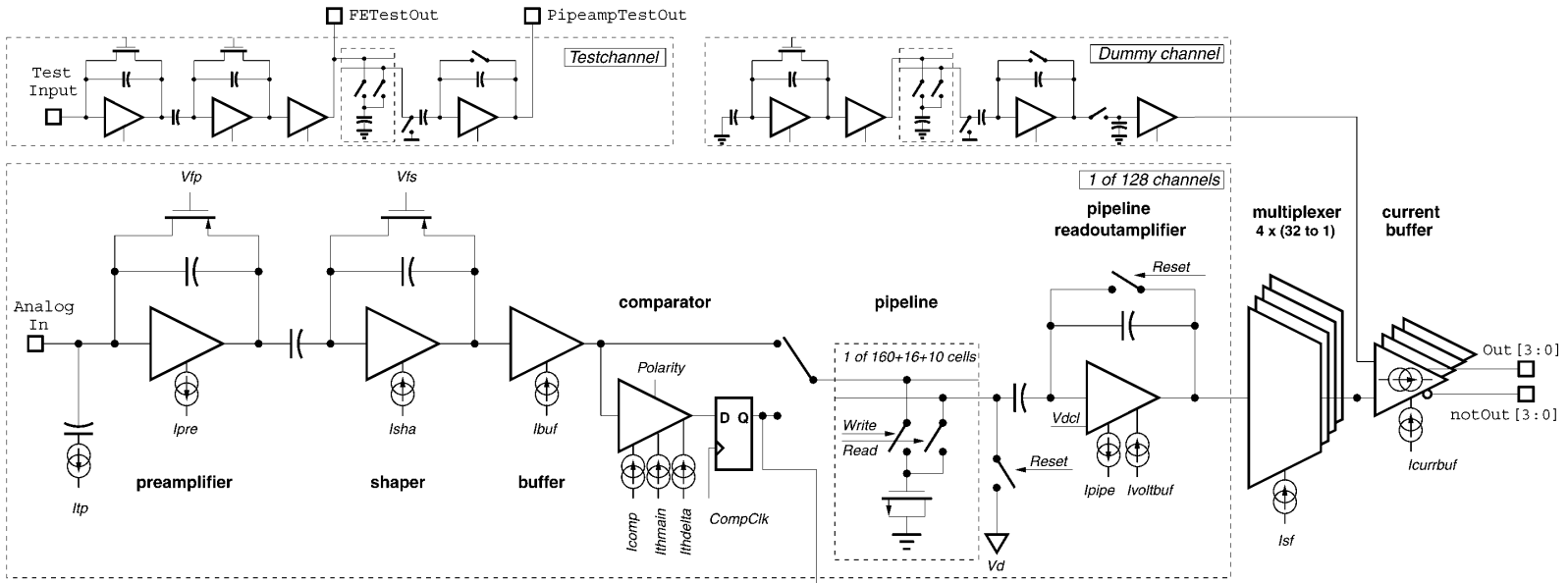
# Beetle: Block Schematic







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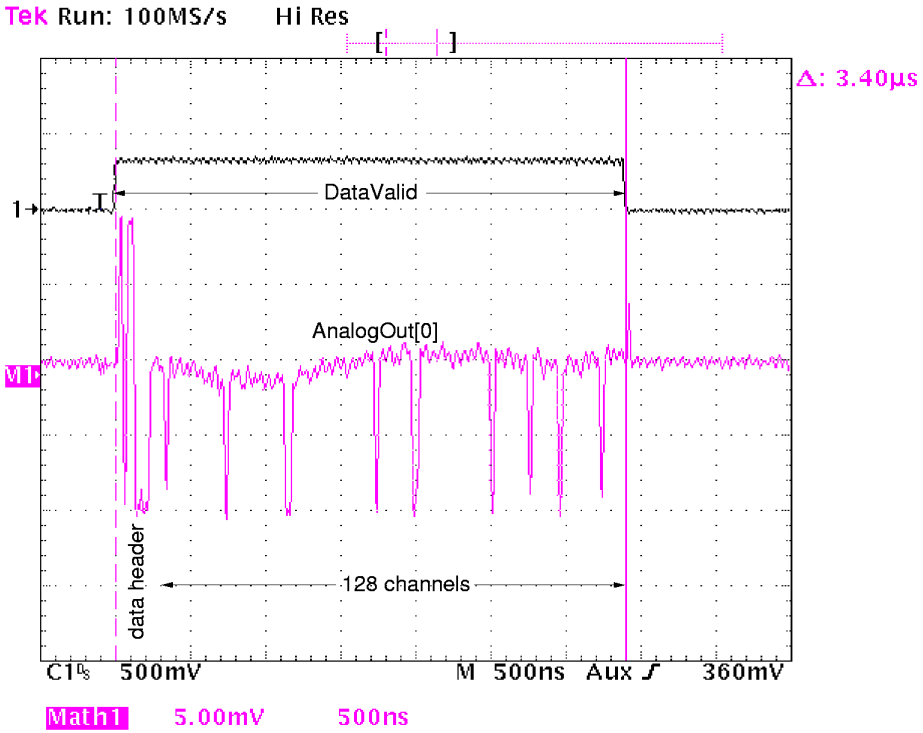
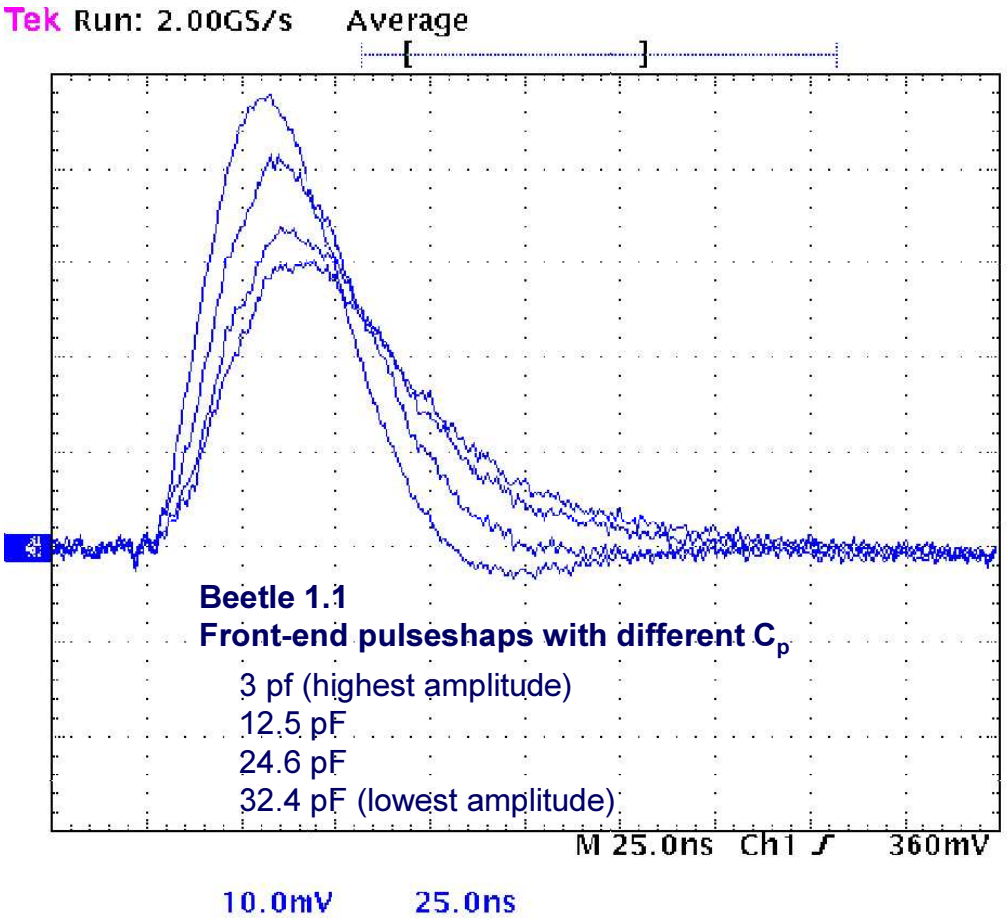
# Analogue readout




**Analogue readout shows the expected behaviour:**

- flat baseline
- correct levels of encoded PCN
- expected front-end gain

# Front end: Pulseshape




**Beetle 1.1**
**Front-end pulseshaps with different $C_p$**

3 pf (highest amplitude)
12.5 pF
24.6 pF
32.4 pF (lowest amplitude)

**Characteristics of Beetle 1.1 FE:**

- peaking time 27 ns
- 30% remainder after 25 ns

- **problems to keep up with LHCb specifications at higher $C_p$**
  *(expected especially for ITR)*
- **input charge rate is limited to 2 nA due to feedback transistor**



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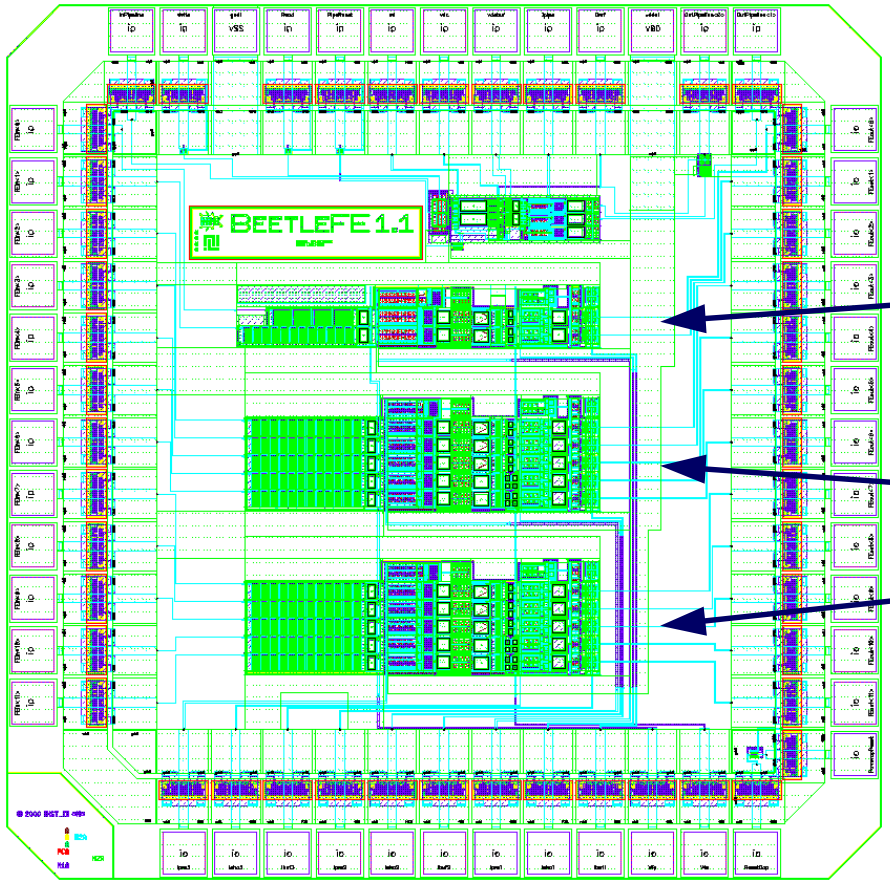
# New front end test chip




Developed a new test chip with modified front ends (submitted 05/2001)

old Beetle 1.0 / 1.1 front ends

2 x 5 new front ends with modified preamplifiers and shapers



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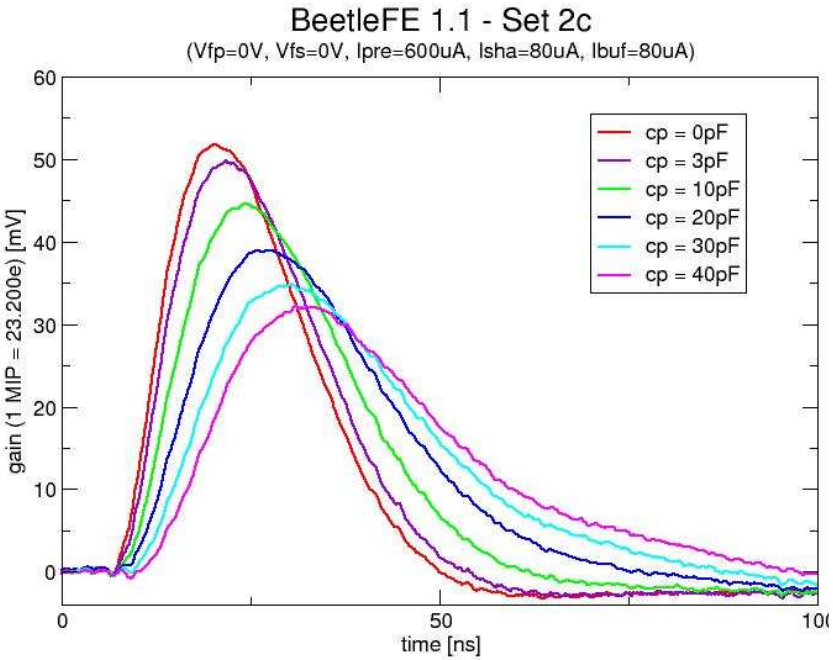
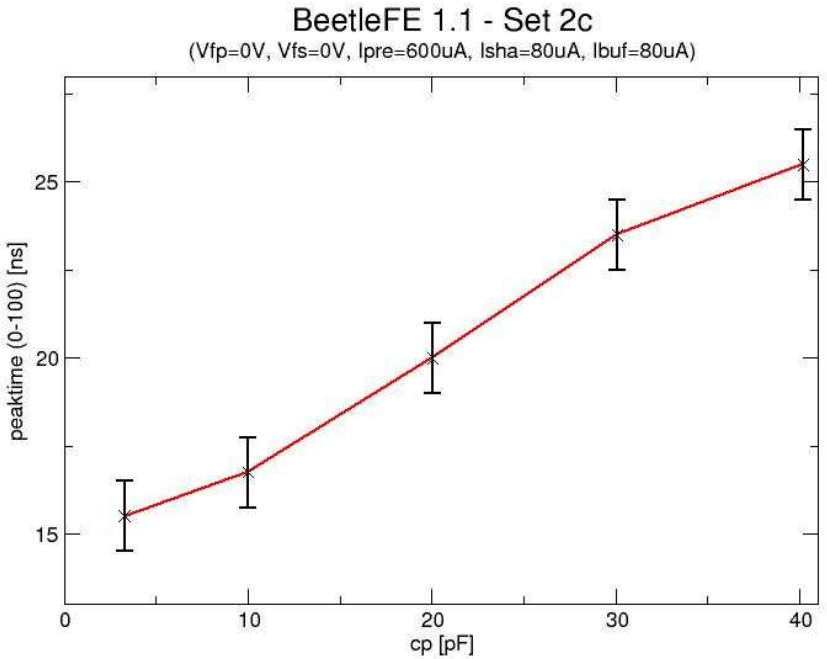
# BeetleFE 1.1: results (1)




**Expected front end behaviour of the new Beetle 1.2**

*(measured on a test chip BeetleFE 1.1. Set 2c )*

- peak-time $\leq$ 25 ns for $C_p \leq$ 40pF



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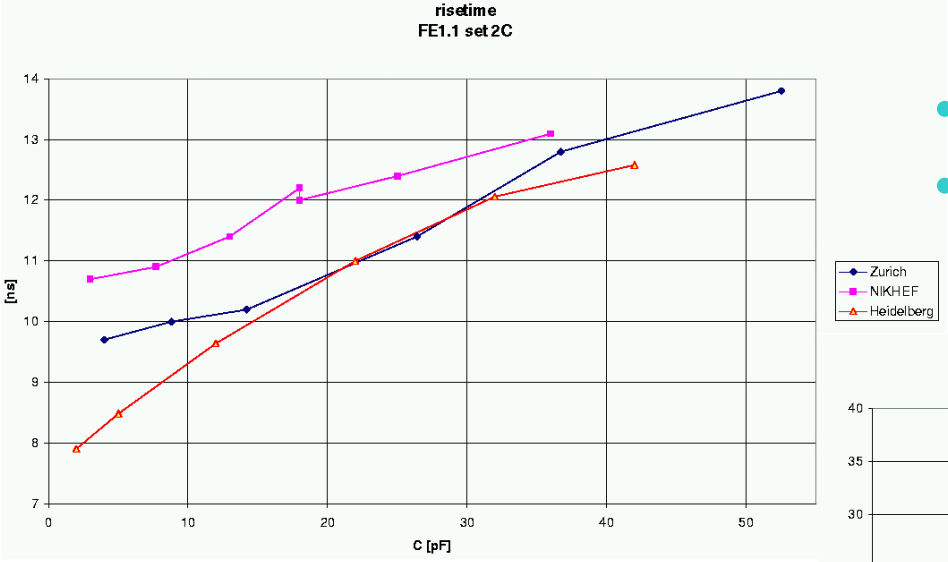
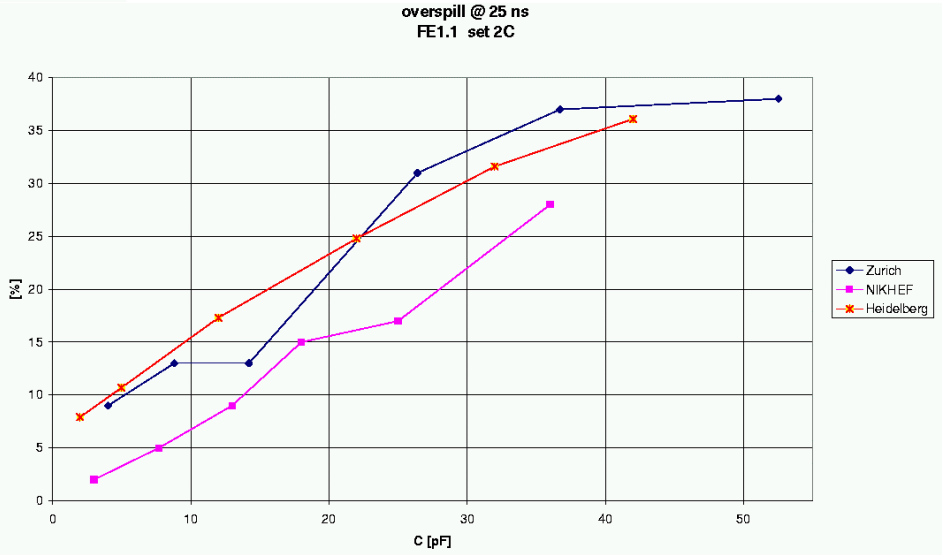
# BeetleFE 1.1: results (2)




- faster rise-time (~13 ns at $C_p$ = 40pF)
- remainder 25 ns after peak less than 30% for $C_p$ < 30pF




## Beetle Front-end Workshop, 7.2.02, HD

⇒BeetleFE 1.1, Set 2c has the best performance and fulfils the LHCb specifications

⇒will be used on the Beetle 1.2



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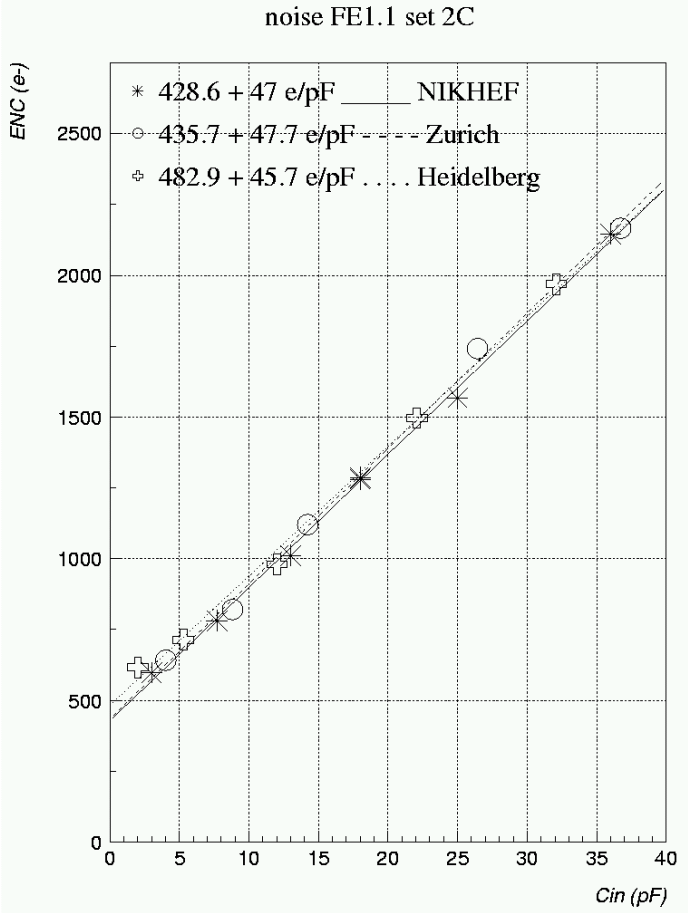
# ENC measurements for new FE




**ENC behaviour of the new Beetle 1.2 front end** *(measured on a test chip BeetleFE 1.1)*:

NIKHEF: 429 $e^-$ + 47.0 $e^-$/pF
Zurich: 436 $e^-$ + 47.7 $e^-$/pF
Heidelberg: 483 $e^-$ + 45.7 $e^-$/pF



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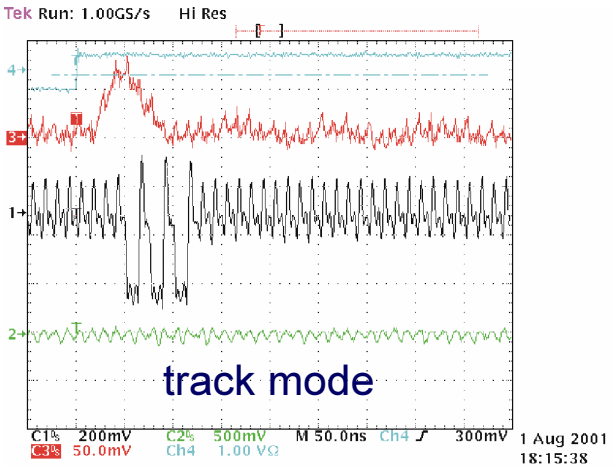
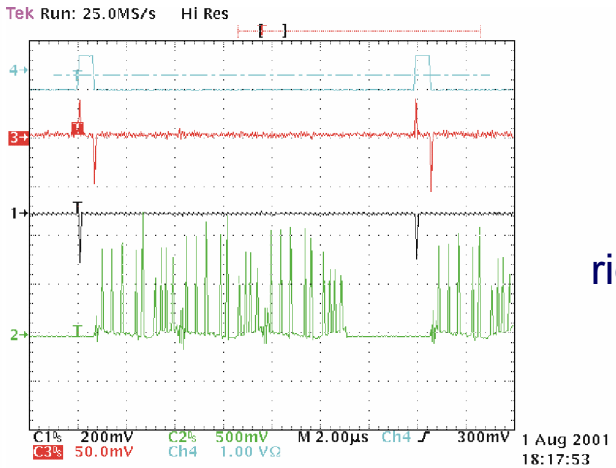
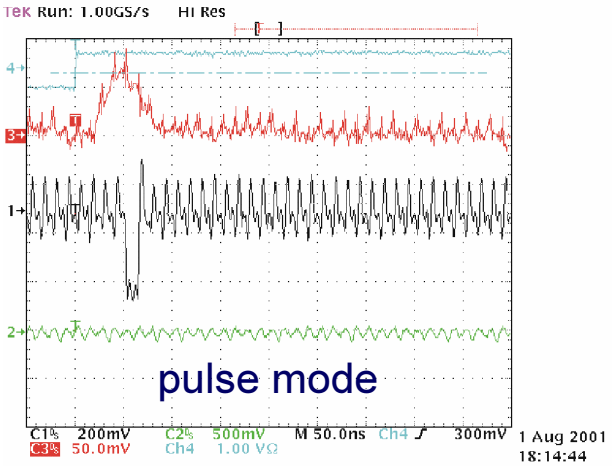
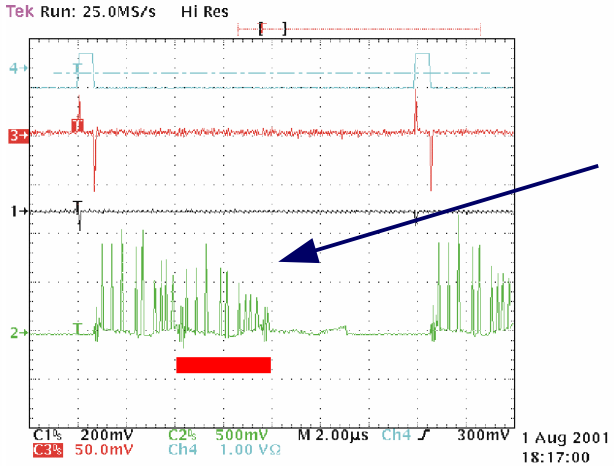
# Comparator




left: - signal pulse shape
- comparator output

right: - binary readout
(4 consecutive BX)

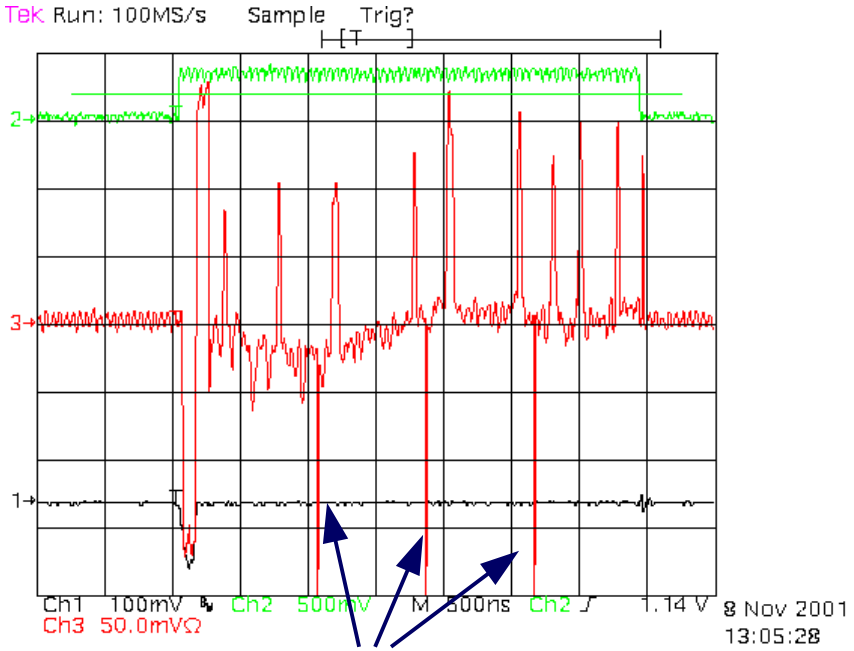
Comparator output level shifter is too slow

⇒ causes spill-over to the second BX

⇒ Beetle 1.2: has now an output buffer

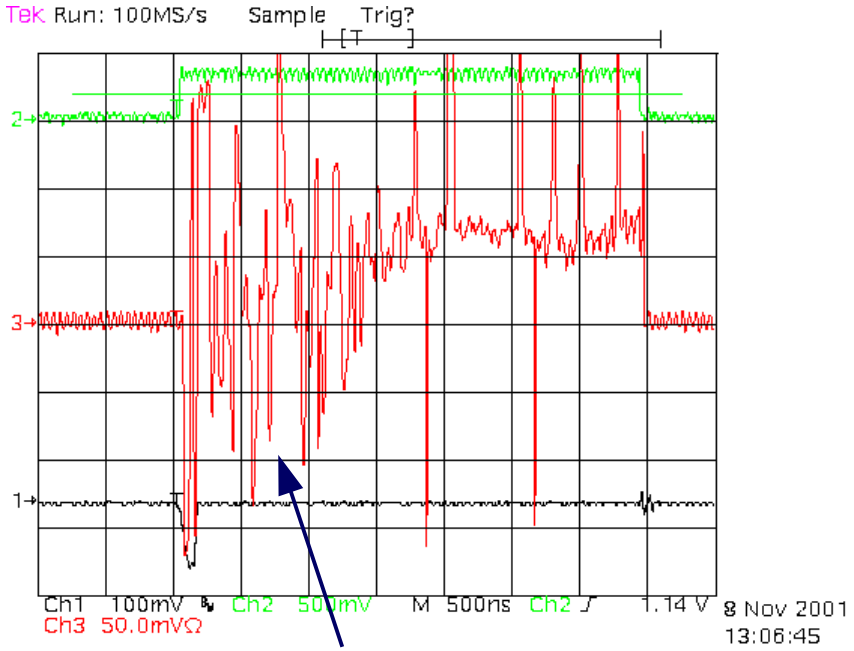
# Pipeamp / Multiplexer

## Readout at trigger rates of 10 Hz and below:




Occurs only in 128 channels on 1 port output mode

⇒ is fixed in Beetle 1.2




Floating wire between Pipeamp and MUX

⇒ wrong DC operation point at the beginning of a readout

⇒ is fixed in Beetle 1.2



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# Beetle 1.1 Control Logic

- Beetle 1.1 processed $10^{12}$ random triggers correctly
  different tests with effective trigger rates between 100 kHz and 1.2 MHz

## Known limitations:

- **"Soft-Reset" feature:**
  applying a "Soft-Reset" at a certain time during readout lets the control logic getting stuck due to a not resetted part of the fast control logic
  $\Rightarrow$ is fixed in Beetle 1.2
- **Trigger-Phasing:**
  bad trigger to clock phasing can violate internal setup times which stops the logic
  $\Rightarrow$ is fixed in Beetle 1.2
- Daisy-Chain *(additional operation mode for test setups)*:
  was not completely implemented in pervious Beetle versions (1.0 / 1.1)
  $\Rightarrow$ is fixed in Beetle 1.2



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# Total Ionizing Dose irradiation

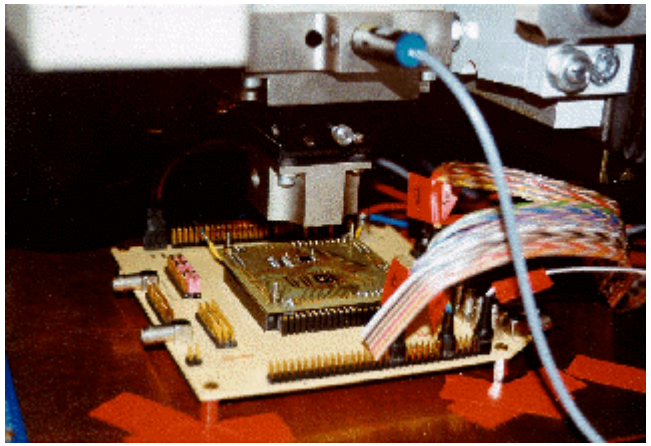
**Done at the X-ray facility of CERN's Microelectronic Group**

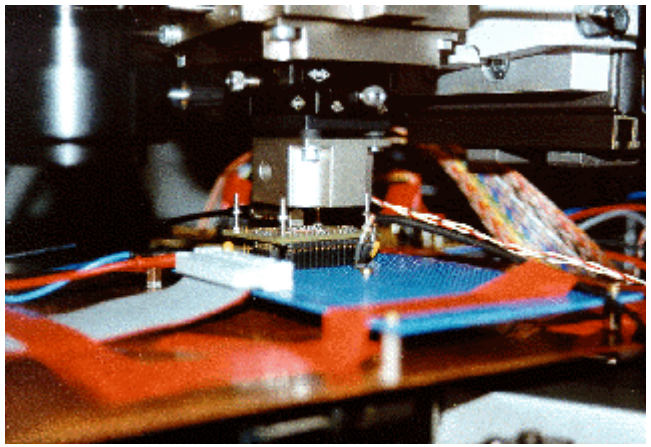
## Irradiated Chips:

- **4 Beetle 1.1 chips**
  - 2 chips being kept at room temperature
  - 2 chips being annealed at 100 °C
- **2 BeetleFE 1.1 chips**
  *containing FE prototypes with a NMOS input transistor*
- **2 BeetleFE 1.2 chips**
  *containing FE prototypes with a PMOS input transistor*

## Accumulated Dose:

- **Beetle 1.1:** 10 Mrad, 10 Mrad, 30 Mrad, 45 Mrad
- **BeetleFE 1.1:** 10 Mrad
- **BeetleFE 1.2:** 10 Mrad







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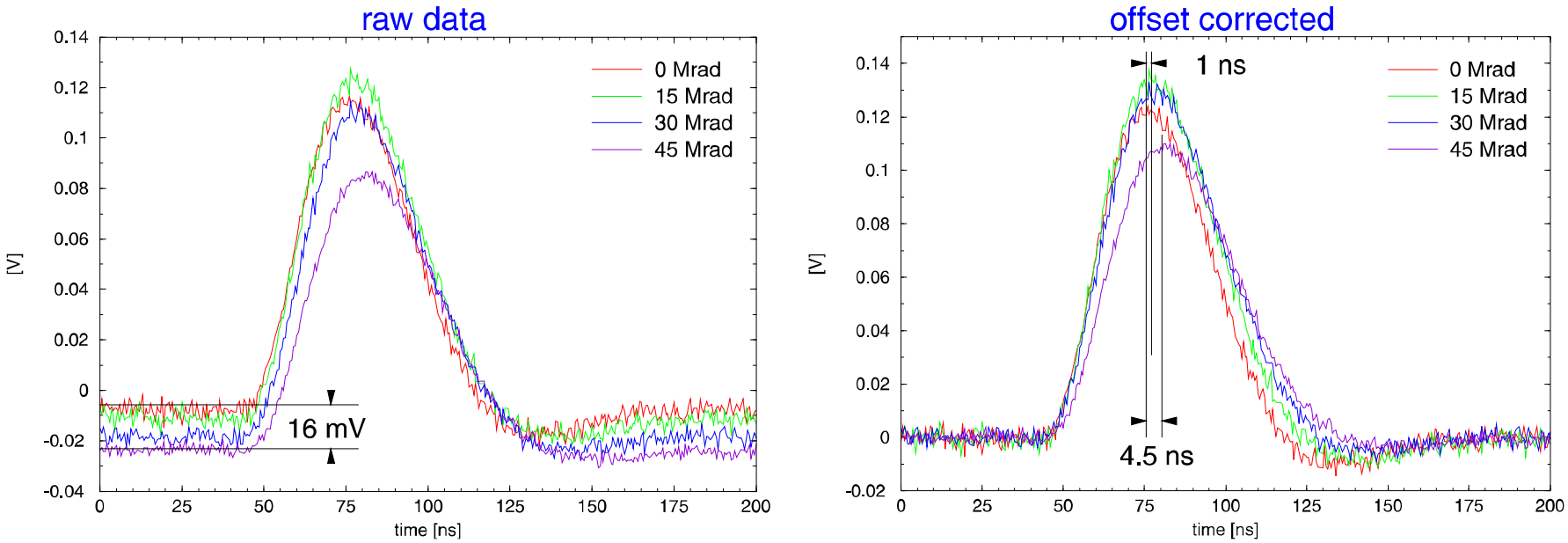
# TID: Results of Beetle 1.1 (1)

## Beetle 1.1 showed full functionality up to 45 Mrad

- full trigger / readout functionality
- full slow control functionality
- performance degradations are small



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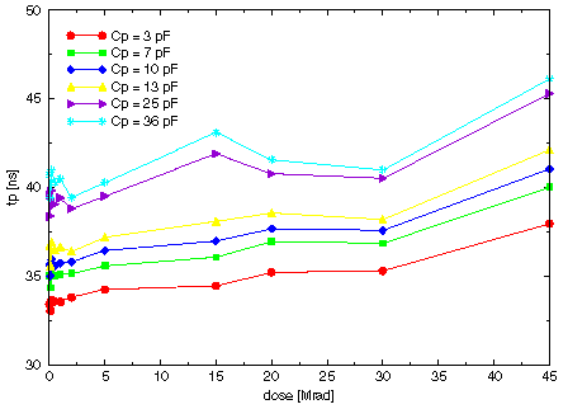
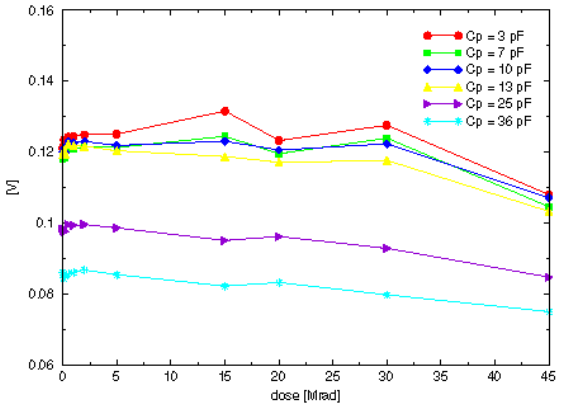
# TID: Results of Beetle 1.1 (2)

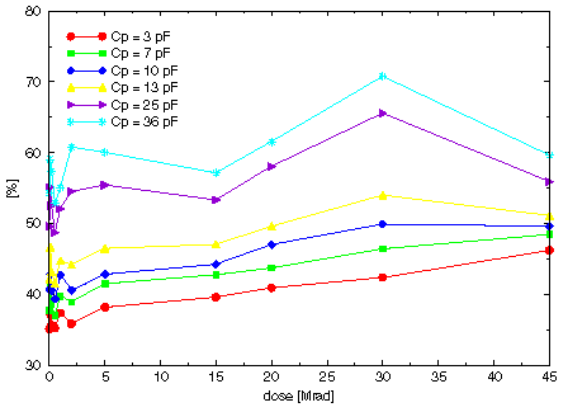
peaking time



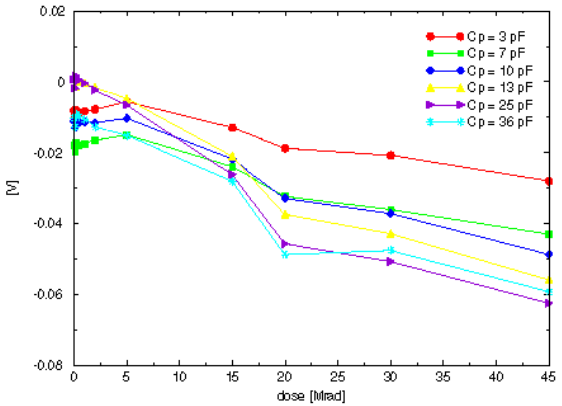

peaking voltage




remainder after 25 ns




offset voltage



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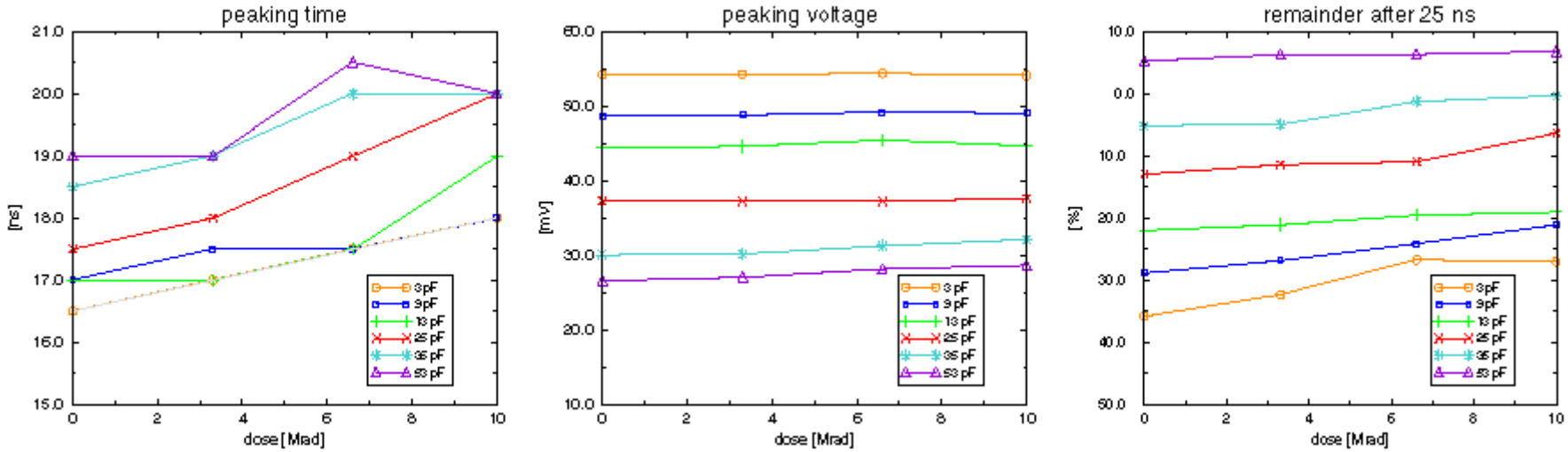
# TID: Results of BeetleFE 1.1

**only minor performance variations during irradiation**




typical slope: 0.1 ns/Mrad



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# Beetle 1.2 (1)

## Modifications on Beetle 1.2

- New placement of the analogue input ESD structure
- Testpulse
  - new design
  - mask registers to switch on/off each channel
- Front end
  - replaced by a new, tested front end from the BeetleFE 1.1 test chip
- Comparator
  - time-constant now programmable
  - mask registers to switch on/off each comparator
  - new output buffer for binary signals
  - replaced all flip-flops with triple redundant flip-flops and majority encoding
  - modified internal comparator clock-timing schema



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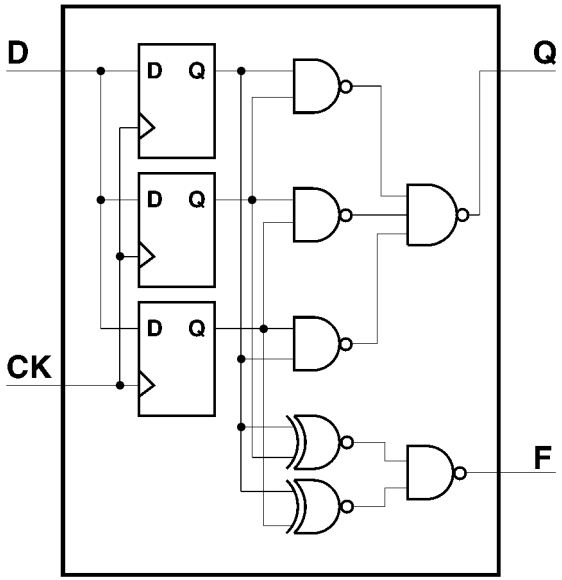
# Beetle 1.2 (2)

- Multiplexer
  - modified MUX control *(to prevent crazy readout at low trigger rate)*
  - all flip-flops are now triple redundant
- Bias / DACs
  - DAC resolution reduced from 10 bit to 8 bit
  - Doubled the max. output current of all current-DACs
  - self triggered, triple redundant flip-flops in all bias registers
- Pads
  - new Beetle Chip Id. pads
  - modified $I^2C$-pads
  - monitoring pads to control both internal current sources
  - 4 additional digital power pads
  - differential analogue output driver with bipolar current



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# Beetle 1.2 (3)

- Slow control
  - hardened against SEU *(state machines use triple redundant flip-flops with majority encoding)*
  - hard wired 7-bit Chip Id.
- Fast control
  - SEU hard
  - new reset schema *(only one external reset and an internal power-up reset for all bias and state registers)*
  - 8-bit SEU counter. Counts all detected and corrected SEU flips.
  - New control schema of the Pipeamp / MUX to prevent the sticky charge problem at low trigger rates.
  - Trigger is latched internally (“Trigger phasing”)
  - Daisy-Chain concept is now implemented
  - New 8-bit analogue readout header *(Start-bit, Parity-bit, EDC status-bit, 3 different parity-bits of registers, 2 LSB-bits of the SEU-counter)*



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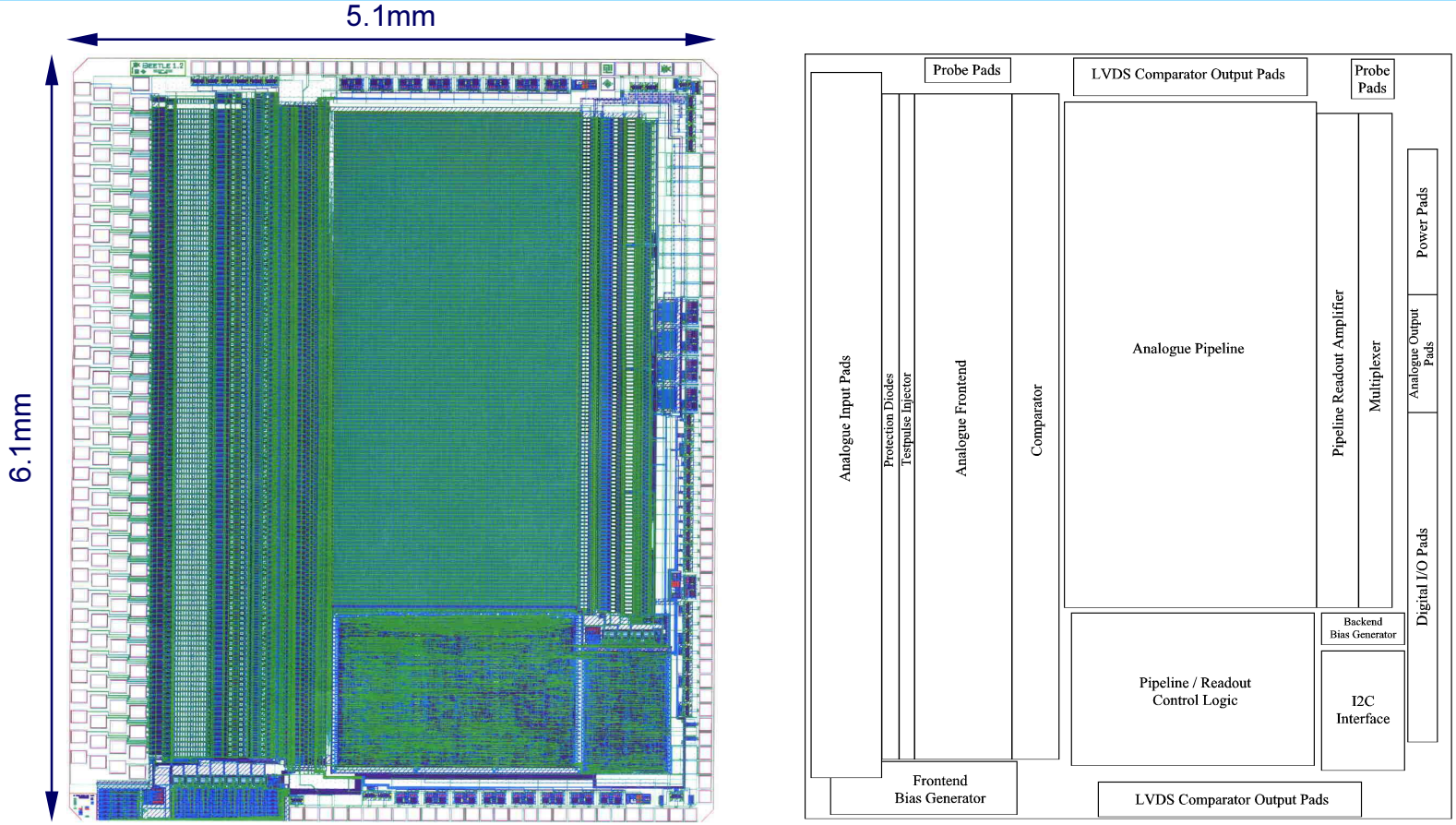
# Beetle: Layout / Floor plan




Layout of the Beetle 1.2 chip and its corresponding floor plan.



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# Next steps / outlook

**Beetle 1.2 is designed to fulfil all LHCb specifications**

**Next steps:**

- Beetle 1.2 is expected back at the end of June
- Lab-test of the Beetle (functionality, readout modes, pulseshape, ...)
- ENC measurements
- TID irradiation test
- SEU test
- ...



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