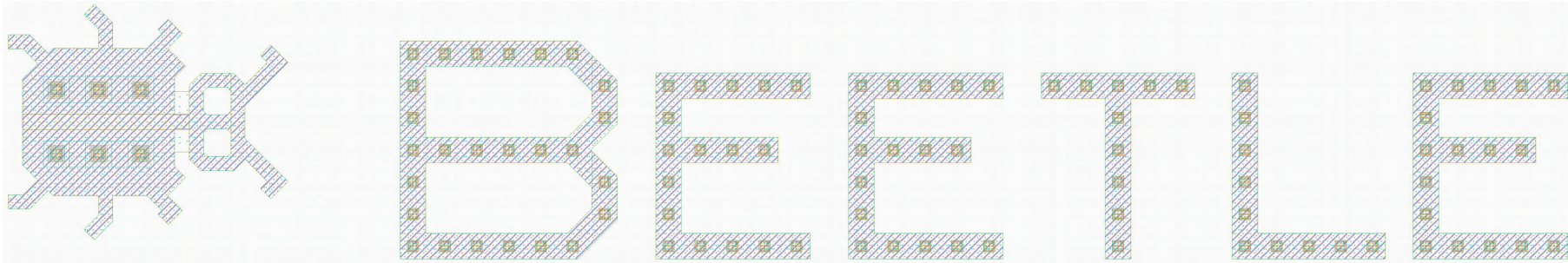


News from



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Beetle 1.1: Test Results

- ☺ Chip is programmable via I²C
- ☺ All on-chip registers can be read back via I²C
- ☺ All readout modes (32→4, 64→2 and 128→1) work
- ☺ Pipeline address (column number) shows correct values and levels
- ☺ Control logic circuits work correct:
 - ☺ WriteMon and TrigMon circulate with the programmed distance
 - ☺ A trigger reduces this distance by one clock cycle
 - ☺ FifoFull becomes active after 16 consecutive triggers
 - ☺ Internal test pulse generator works

- ☺ Pulse Shapes
- ☺ Baseline and control Voltages
- ☺ Comparators
- ☹ Binary Readout

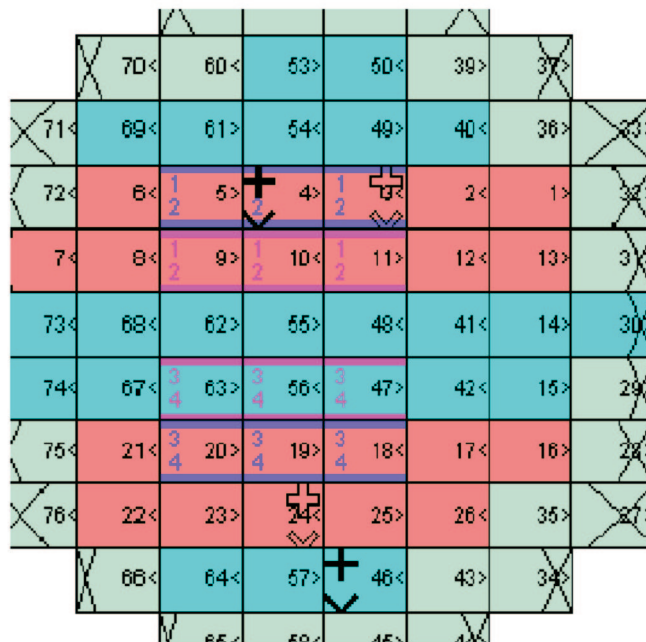
- Not yet tested:
 - ☹ Noise
 - ☹ Comparator threshold

Striping of MPW4

The minimum L_{eff} has been varied across the wafer:

There are strips with -3σ , -1.5σ , 0 , $+1.5\sigma$ and $+3\sigma$

Chips cannot be assigned to those L_{eff} groups



Mapping des stripes en PC sur le produit MPW4 (63F5354) :

Expo en DUV sur Micrascan : Notch right

Field size : 20.038*26.756mm

Chips per field : 2*1

chip size : 19.90*13.00mm

Chips per wafer : 92

Field 1-6 : 85% of nominal dose

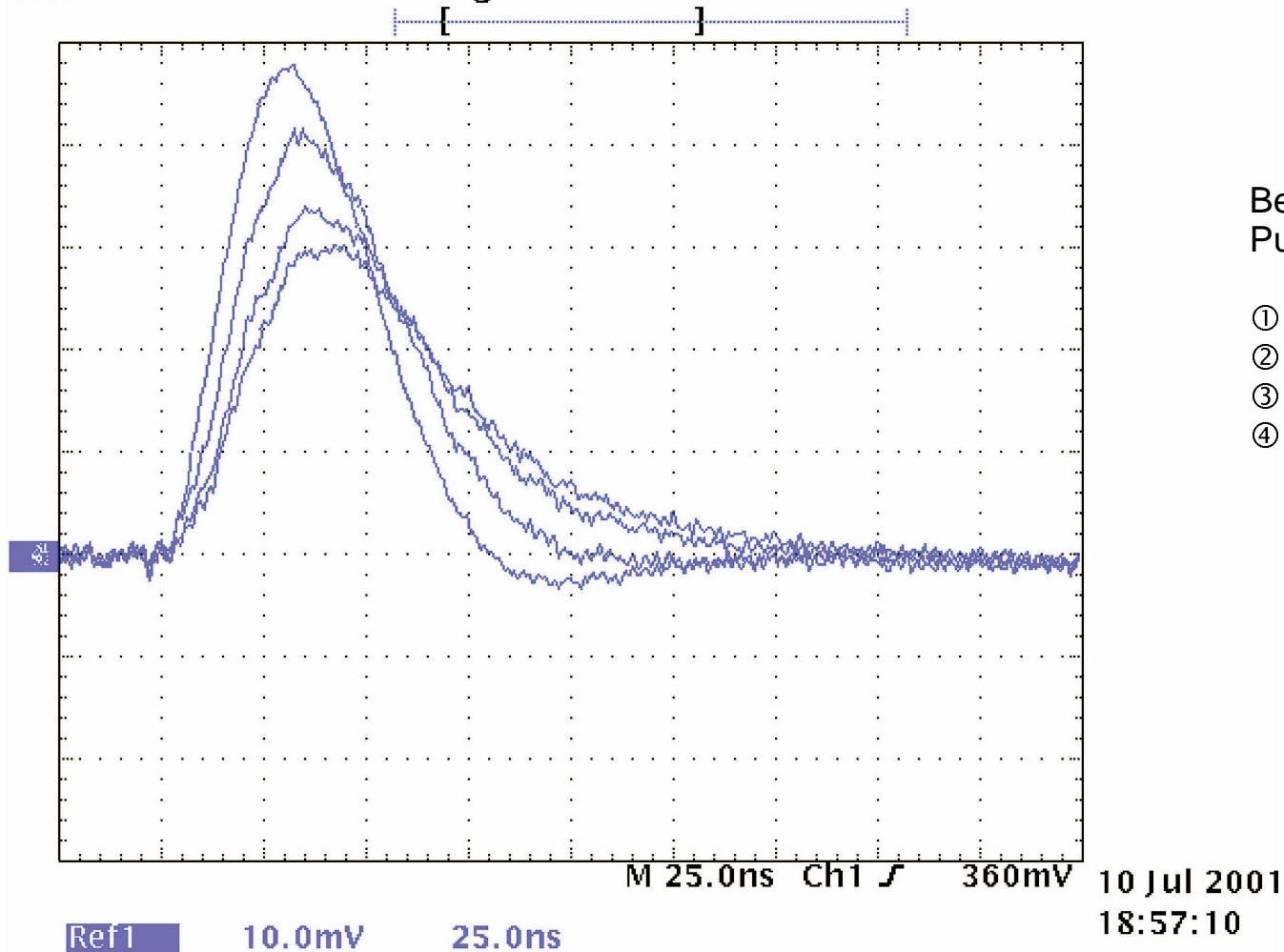
Field 7-13 : 92%

Field 16-21 : 115%

Field 22-26 : 125%

Beetle1.1: Pulse Shapes I

Tek Run: 2.00GS/s Average



Beetle 1.1
Pulse shapes of the test channel:

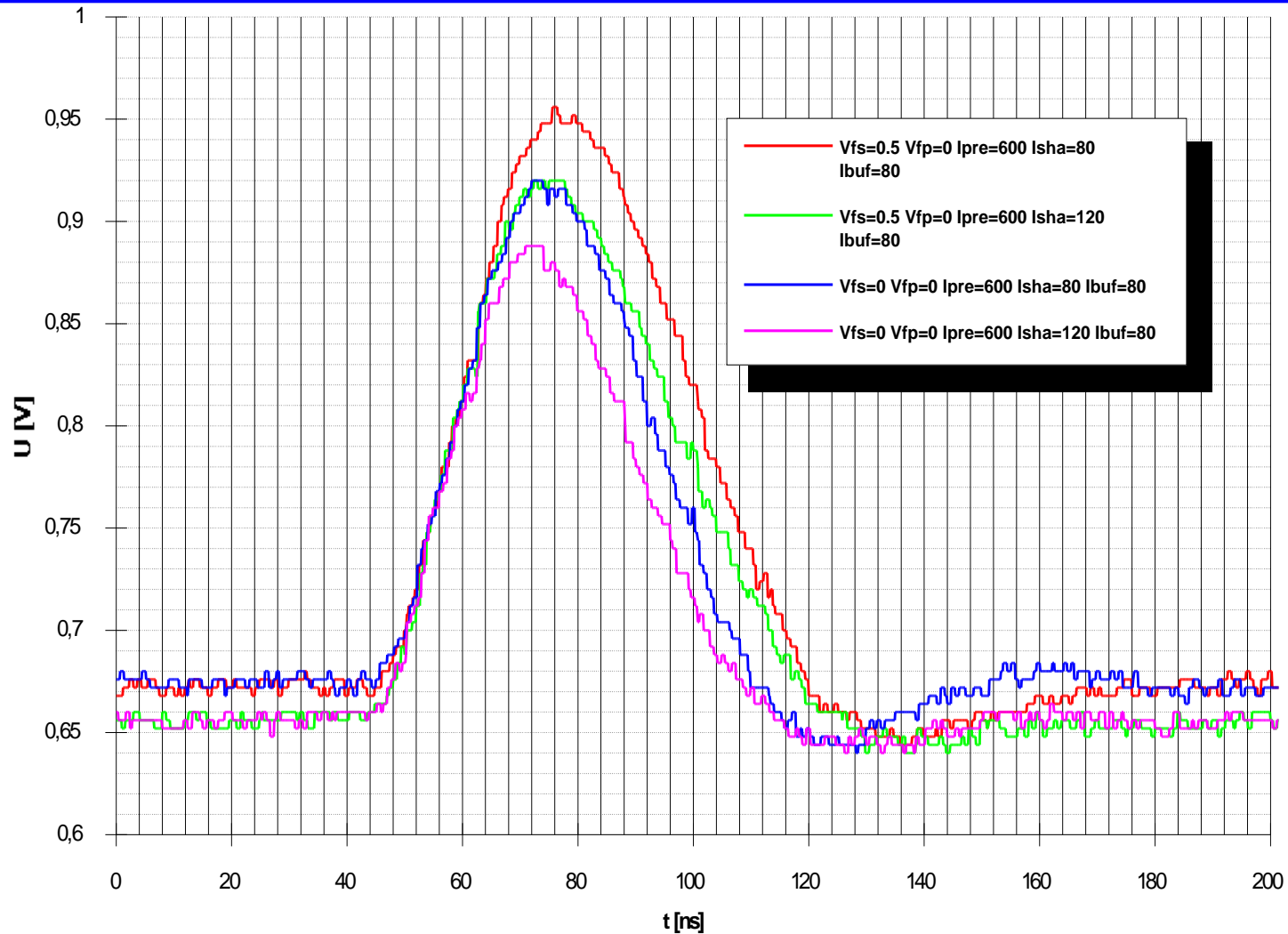
- ① 3pf (highest amplitude)
- ② 12.5pf
- ③ 24.6pf
- ④ 32.3pf (lowest amplitude)

Beetle1.1: Pulse Shapes II

Comparison of NIKHEF and Heidelberg measurements

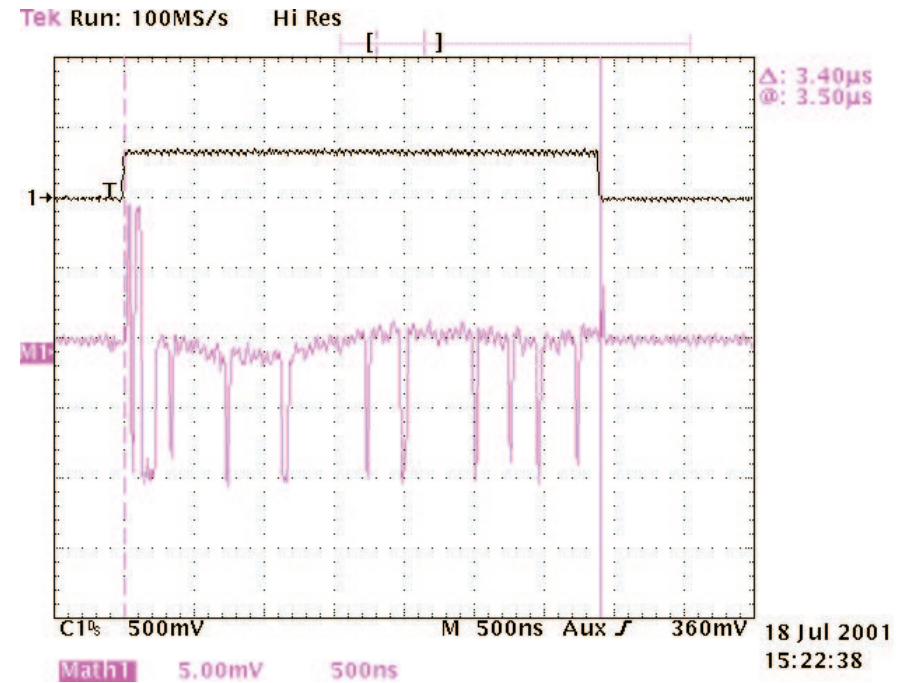
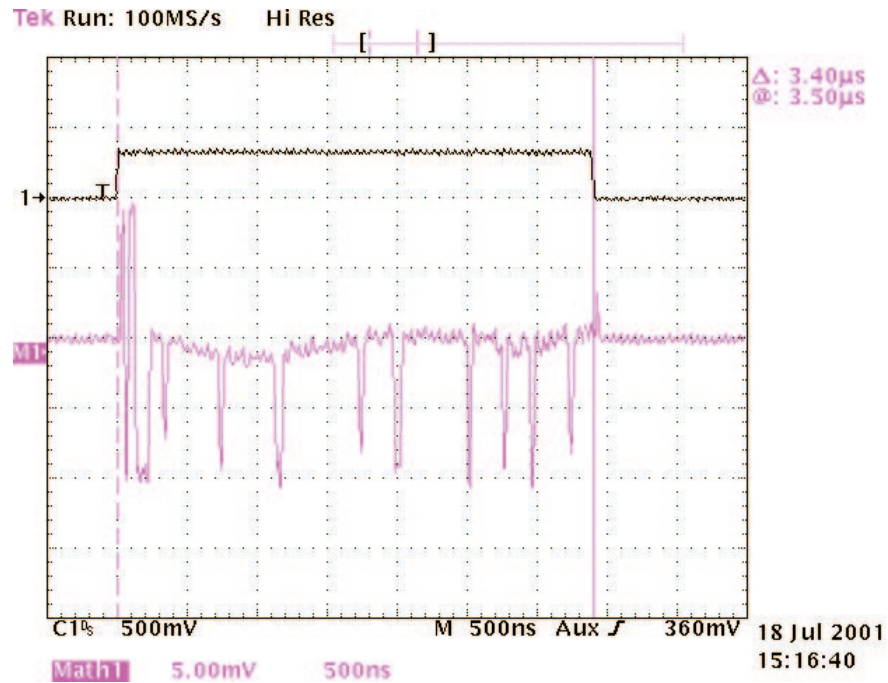
FE parameters					BeetleCO10 (NIKHEF)			Beetle11: test channel (Heidelberg)			
Vfs [mV]	Vfp [mV]	Ipre [μ A]	Isha [μ A]	Ibuf [μ A]	$t_R^{10/90}$ [ns]	spill-over [%]	Vpeak [mV]	$t_R^{0/100}$ [ns]	$t_R^{10/90}$ [ns]	spill-over [%]	Vpeak [mV]
0	0	425	87.5	200	14.5	27.4	20.8	26.5	19.0	31	17
0	0	500	50	200	16.0	18.3	22.7	29.5	22	35.5	18
0	0	500	163	200	15.0	28.8	19.1	24	17.2	39.2	15.8
0	375	500	87.5	125	16.5	29.1	19.5	26.0	19.2	30.8	16.2
0	375	500	87.5	200	14.5	21.2	20.8	25.5	19.7	33.7	16.6
0	1125	500	50	200	17	20.1	18.8	30	22.0	37.7	12.2
0	1125	500	87.5	200	14.5	25.6	17.5	25.0	19.2	32	11.8
0	1500	500	87.5	200	16.0	22.4	18.1	25.2	18.7	32.8	11.6

Beetle1.1: Pulse Shapes III

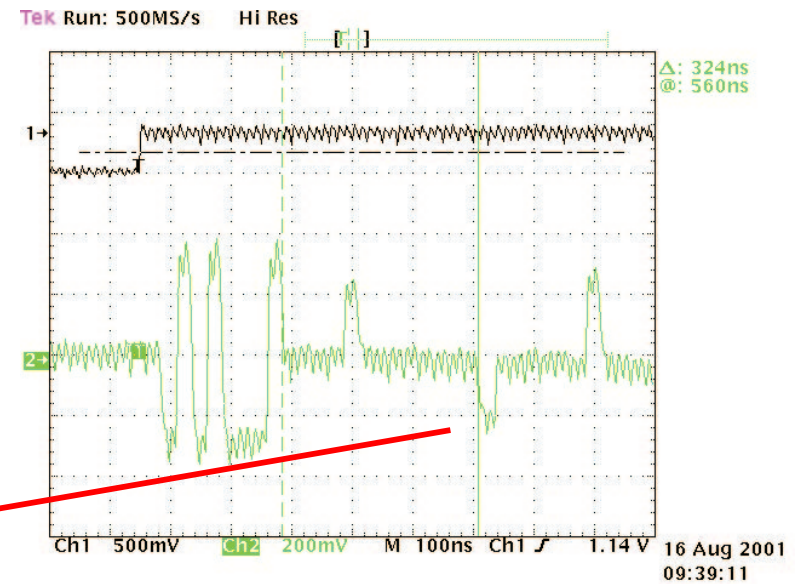
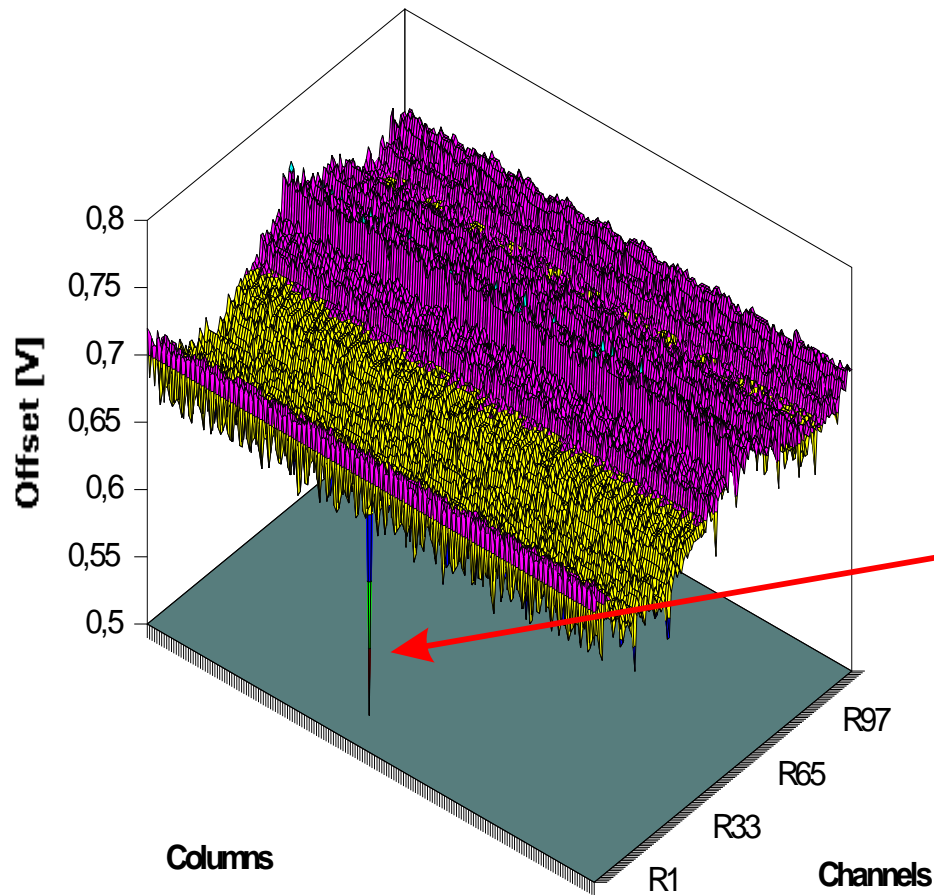


Beetle1.1: Optimized Settings

Optimized settings for V_d and V_{dcl} result in a flat baseline

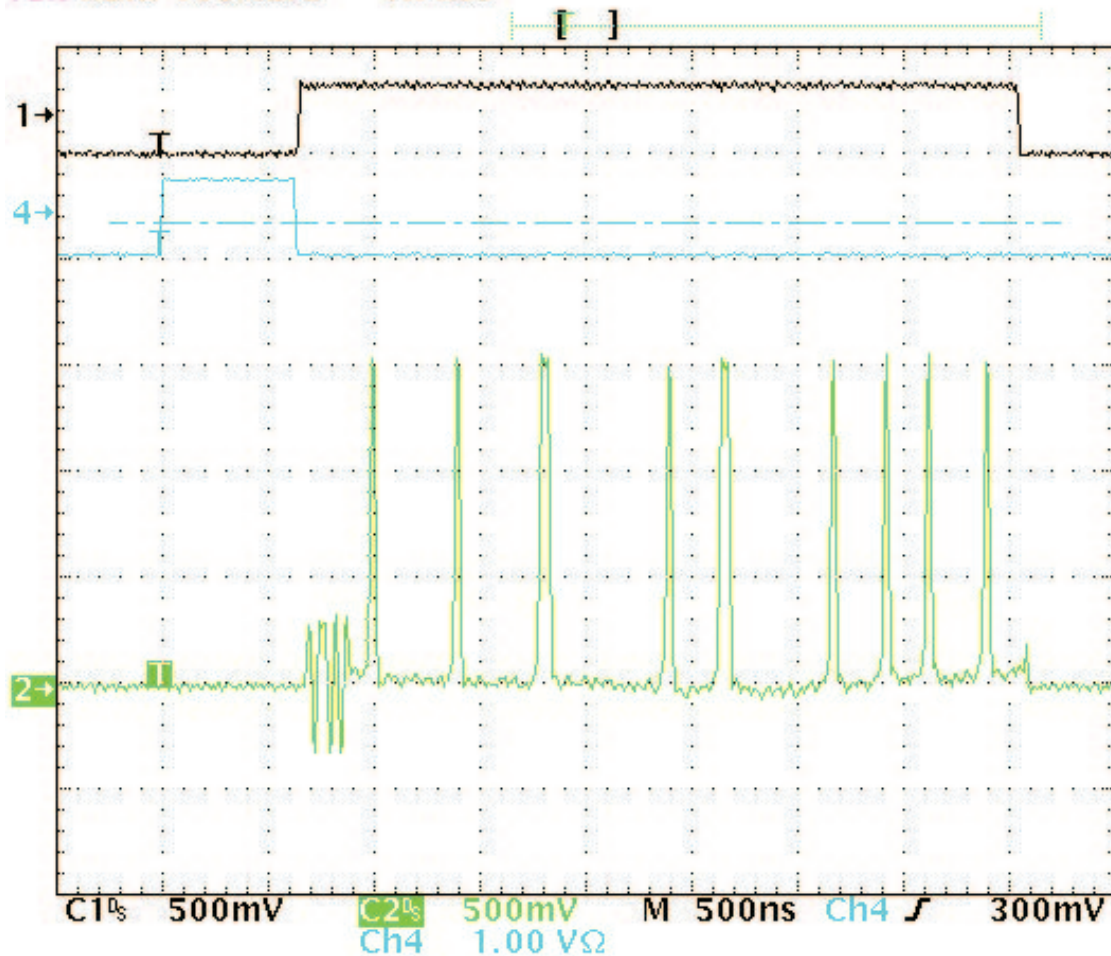


Beetle1.1: Pipeline Scan



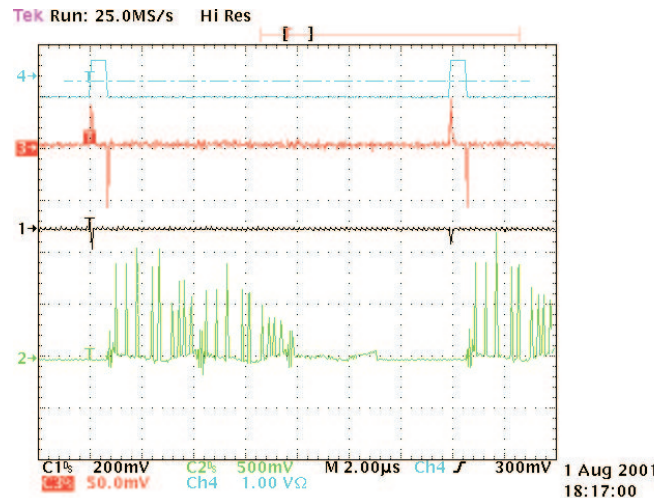
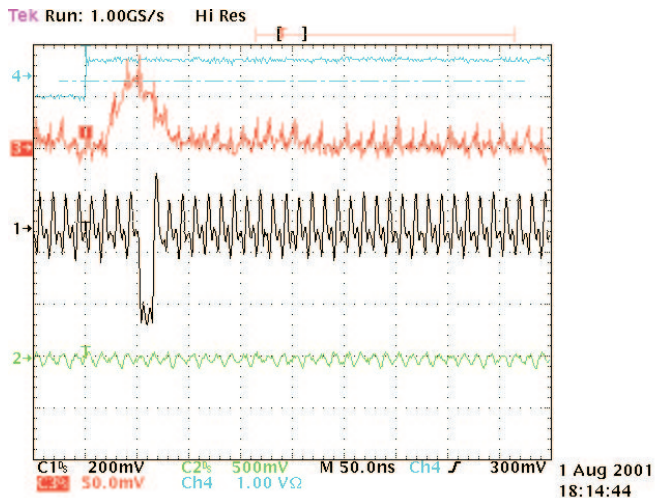
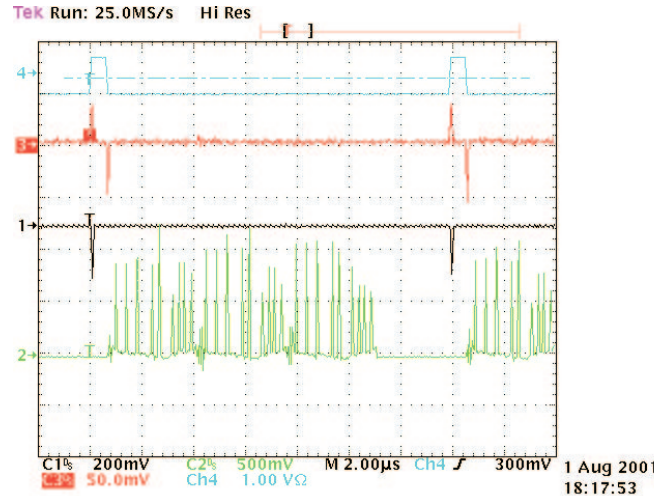
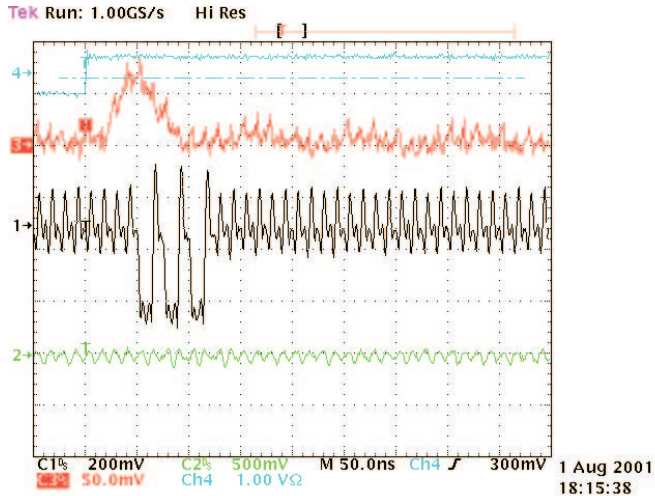
Beetle1.1: Binary Readout

Tek Run: 100MS/s Hi Res



- ☺ Binary readout mode works
- ☺ Levels are 0 and +10 MIP (as designed)
- ☹ Phase of CompClk and Clk has to match (latched comparator output is sampled)
- ☹ but...

Beetle1.1: Comparators



- ☺ track mode (top)
- ☹ pulse mode (bottom)
- ☺ Comparator outputs (left)
- ☹ Binary readout (right)

➔ Level shifter is too slow causes spill-over to the second BX



Beetle1.1: Outlook

Bugs found:

- Frontend too slow and too low rate capability (known)
- Voltage divider for binary readout too slow

Still to be measured:

- Noise (PCB for that purpose is ready)
- Comparator threshold and crosstalk
- New BeetleFE and BeetleSR chips (which arrived last week)

