Status of OTIS

Outer Tracker Time Information System

LHCb Week Rio

2001, Sept.17 – Sept. 21

OTIS GROUP, Heidelberg University

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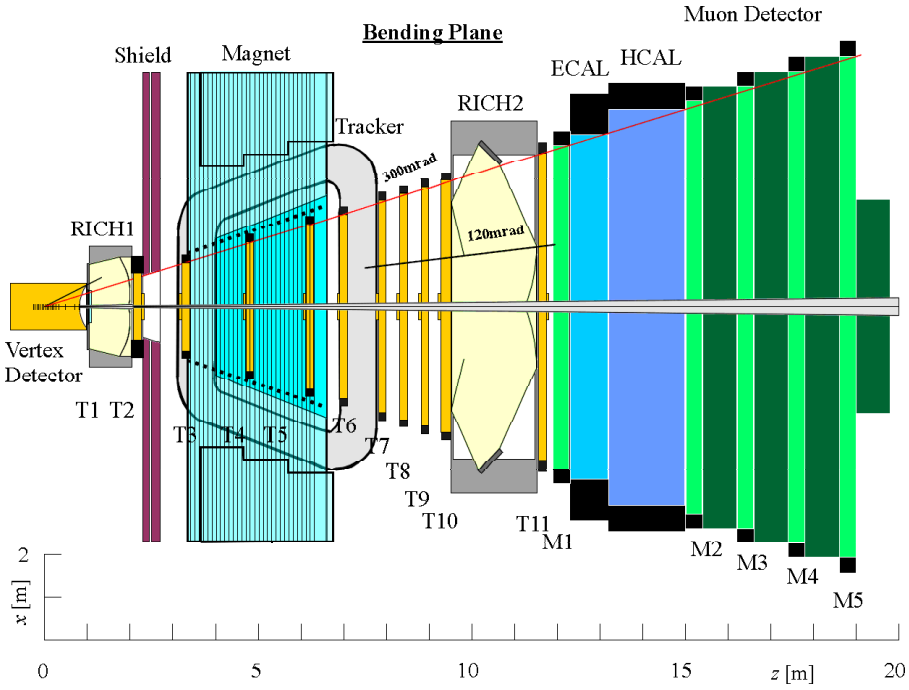
LHCb at Cern

Cern

LHCb



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OTIS TDC

Outer Tracker Time Information System

- 3.250 OTIS-TDCs with
  32 channels each
- 4 OTIS TDCs are connected to one GOL
  fast serializer ⇒ one fibre per 128 channels
- Radiation hard layout 0.25 µm
- DLL fine time resolution 6 bit
- Dual Ported Memory with 1.2 Gb/s,
  240 bit width ⇒ low power design
- Synchronous clock driven readout

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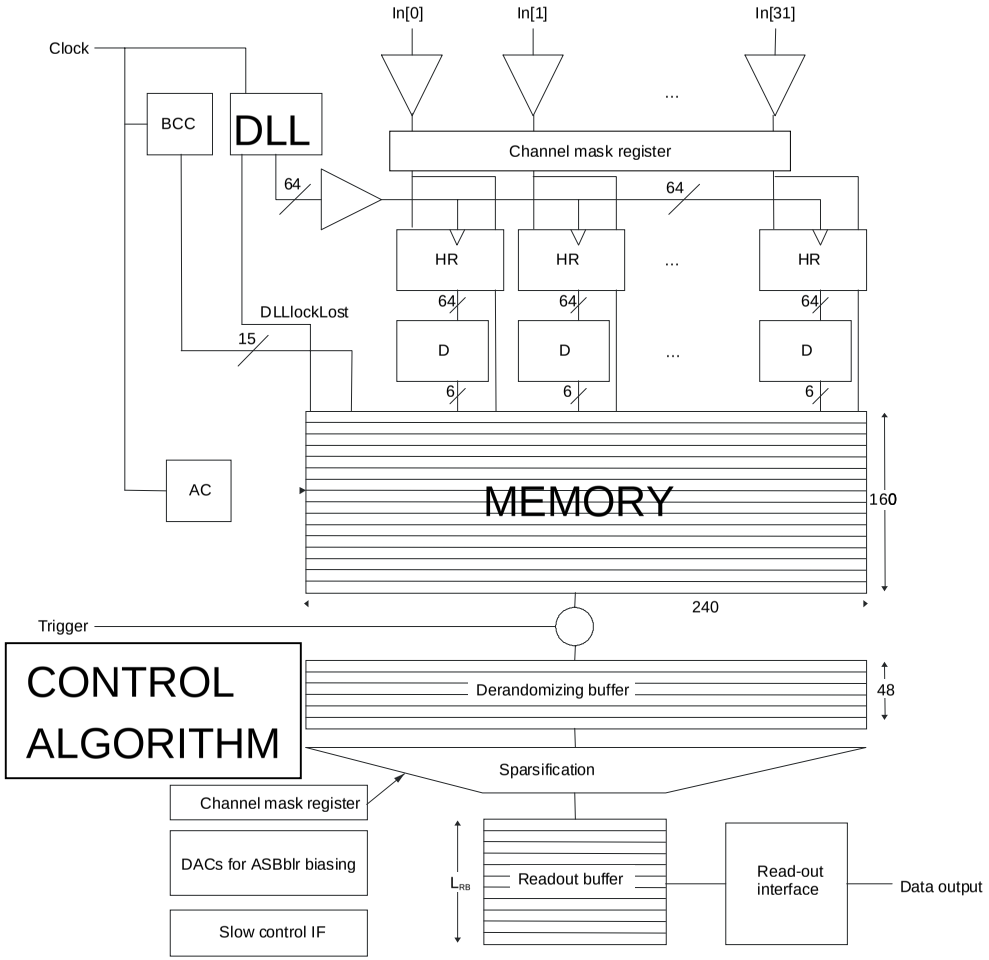
LHCb OTIS TDC



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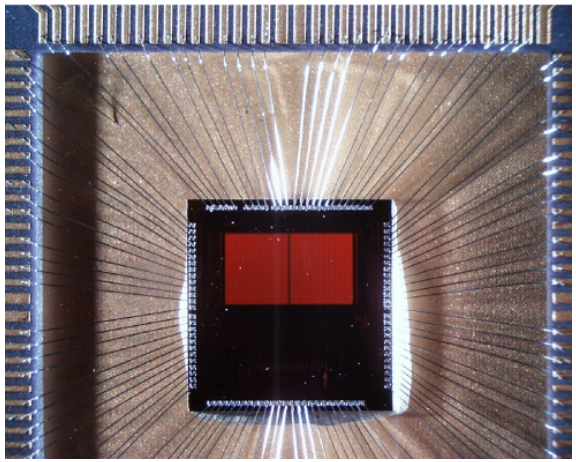
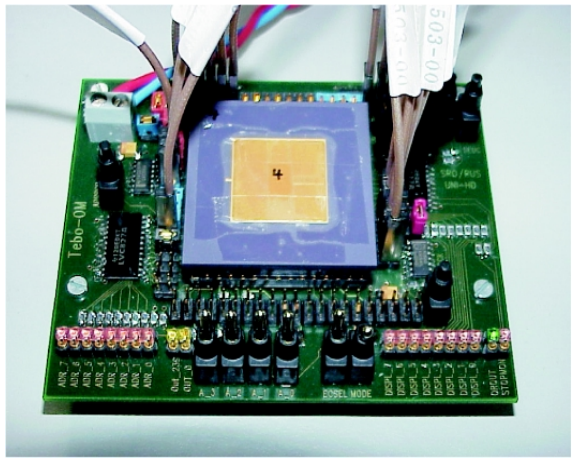
Delay Locked Loop

Test chip for MEMORY and DLL with MUX: OTISMEM1.0, submitted February 2001

Chip OTISMEM1.0 received and tested: Preliminary results available





- 2nd DLL prototype, contains:
  - Delay chain with 32 stages 2 taps each
  - Mean delay per tap 25ns/64 = 390 ps
  - Currently Hit Register
    for only one channel
    with 64 bit multiplexed to 4 pads

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DLL Lock Time

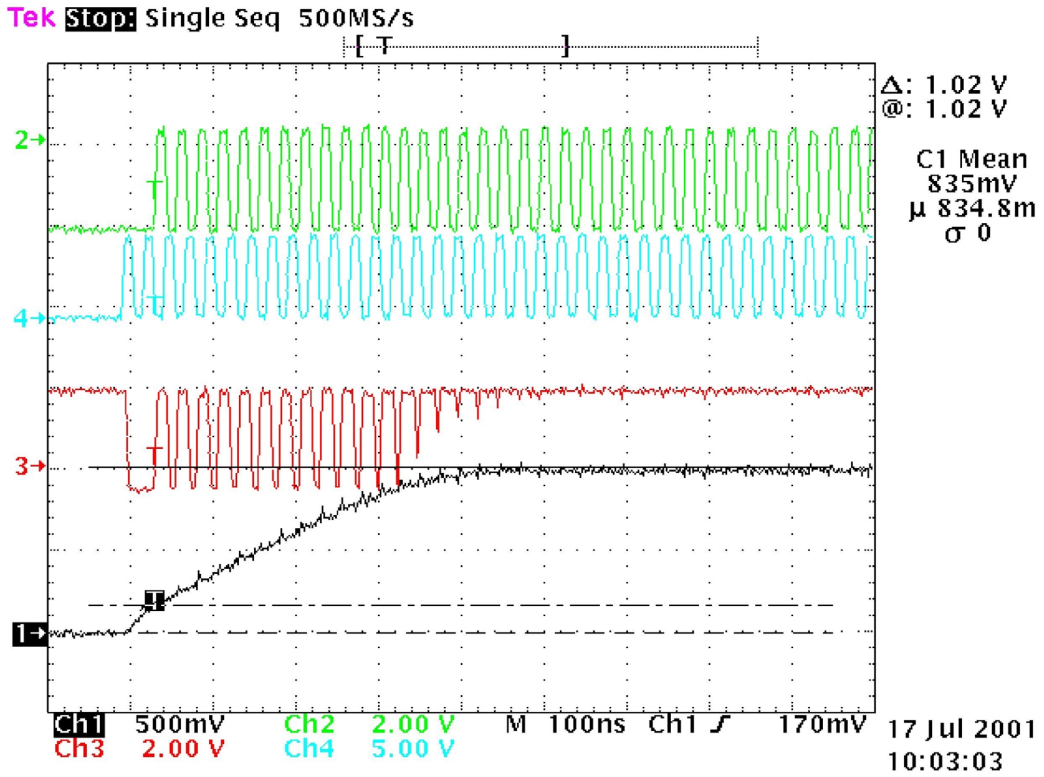
- Lock Time is below 1µs

DLL Out

Clock In

Phase Difference

Control Voltage DLL



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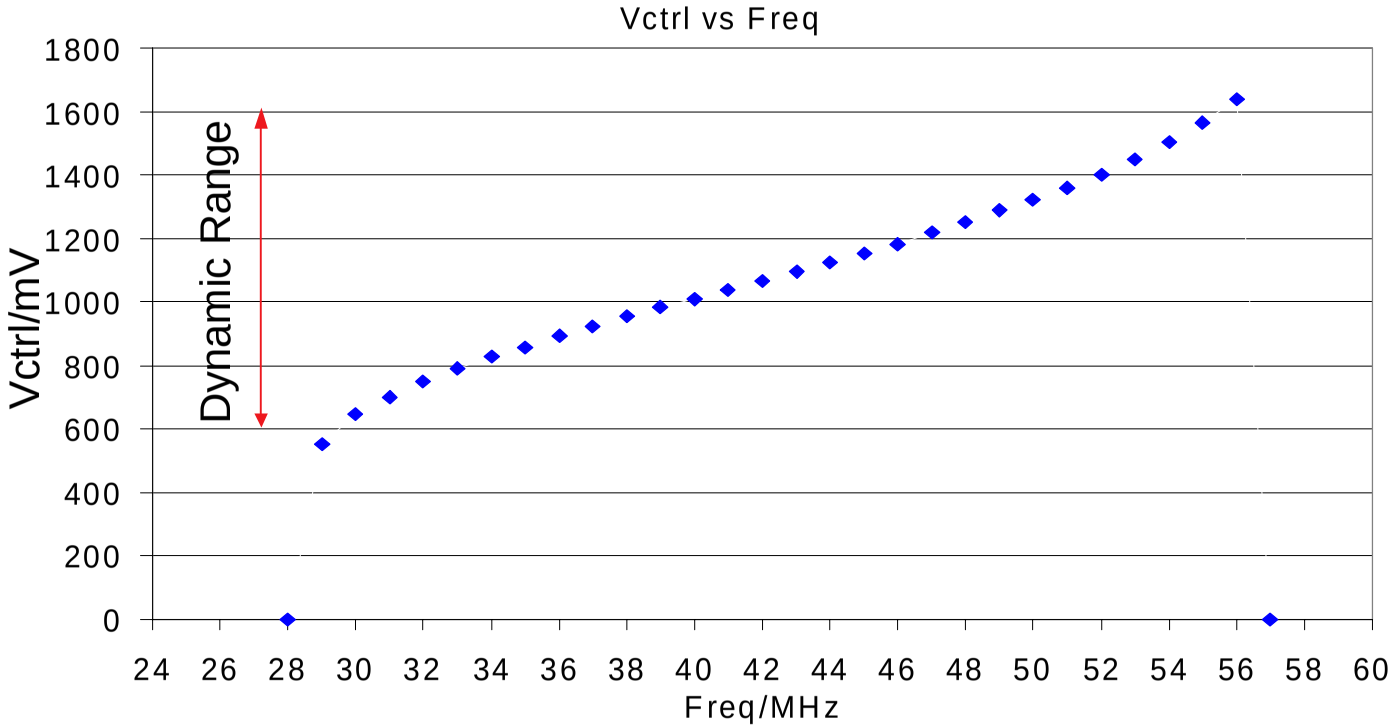
DLL Lock Range

- Lock Range = 29…56MHz at 300K
  - simulated Lock Range 30…50MHz (Within an 10% error)
  - Spec is 30…50MHz at 300K➔ OK !!!
- Dynamic Range of Control Voltage 1V



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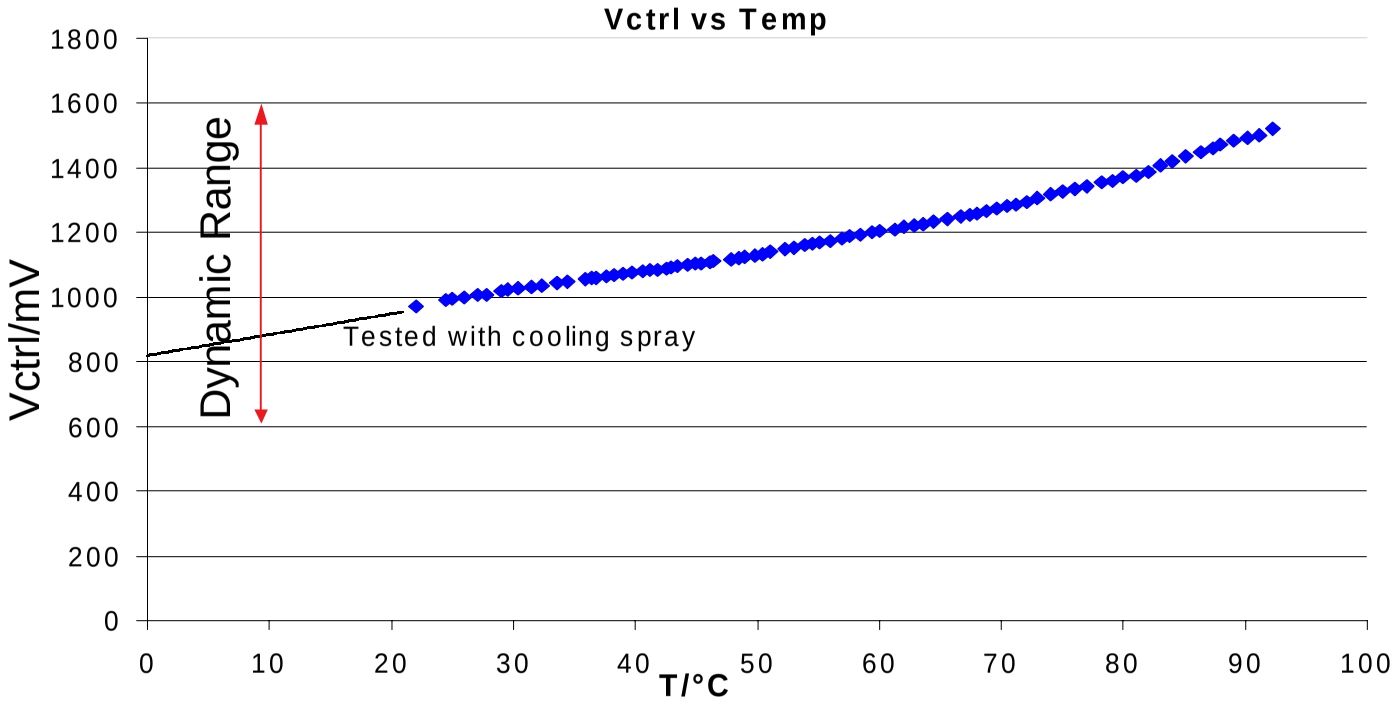
DLL Temperature Range

- Measurement of Temperature Range
- Control Voltage inside Dynamic Range for all tested Temperatures at 40 MHz



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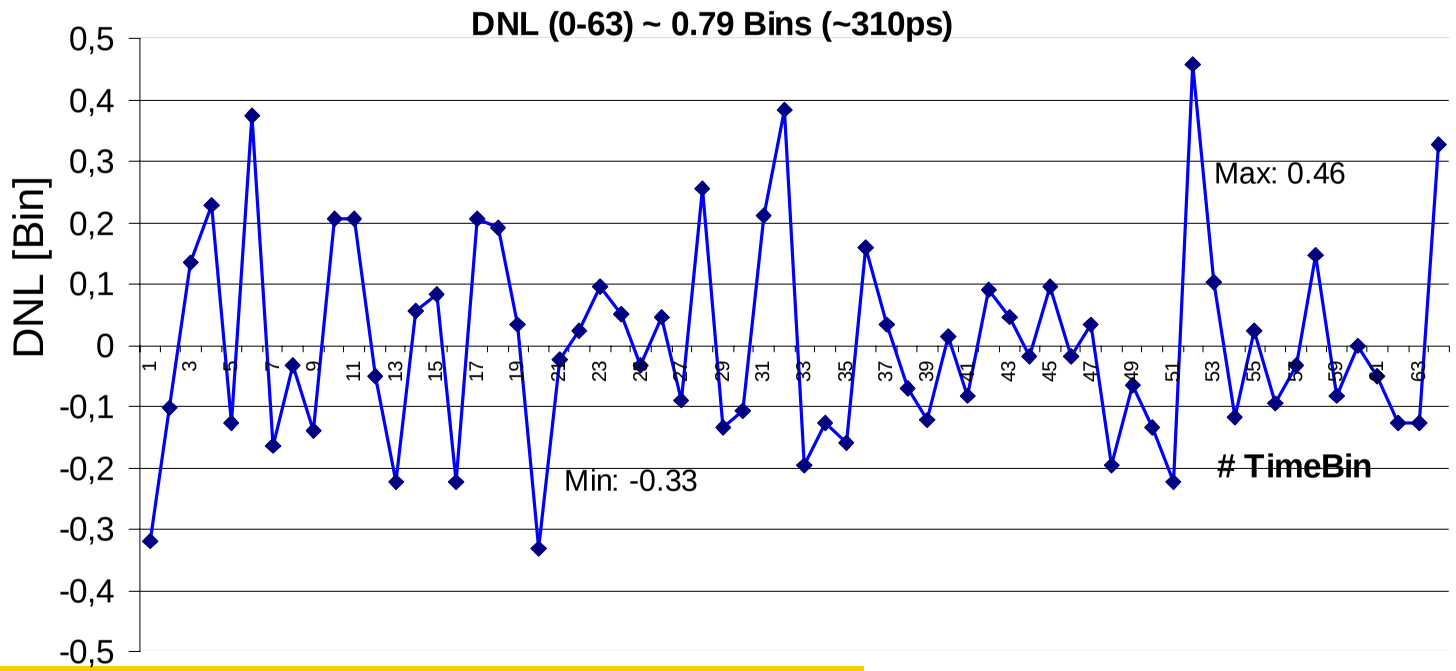
DLL Differential Non Linearity

- Differential Non-Linearity (DNL) preliminary:
  - 0.79bins (~310ps) at 40MHz
  - Influence of MEMORY switching on DLL not tested
  - Influence of test chip specific MUX on DLL⇒Guard Ring cut



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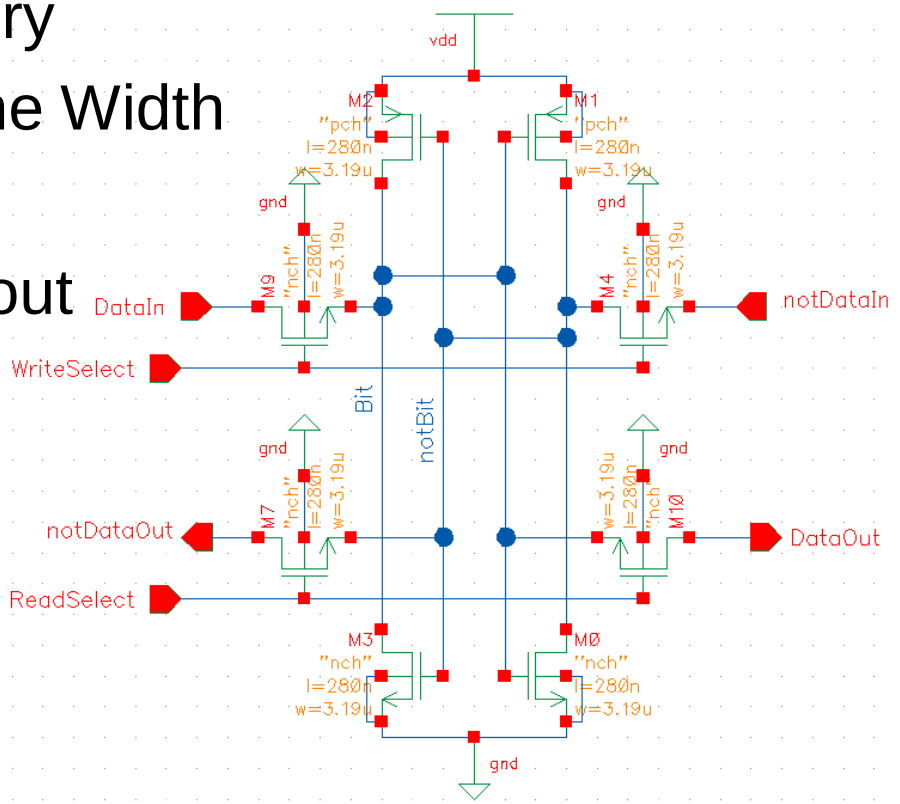
OTIS MEMORY

- Implemented on OTIS MEM1.0
- Dual Ported Memory
- 240 bit total Pipeline Width
- 164 rows long
- Radiation hard layout
- Low power design



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MEMORY Timing

Symbol	Parameter	Simulation		Test chip		Unit
		Best	Worst	Best	Worst	
t_{AVRH}	address valid to read enable high	≥1.5	≥3	≥-0.3	≥-0.3	ns
t_{RLAX}	read enable low to address transition	≥2.5	≥5	≥-0.6	≥-0.3	ns
t_{RHRL}	read enable high to read enable low	≥4	≥8	≥1.6	≥2.1	ns
t_{RLRH}	read enable low to read enable high	≥8	≥15	≥5.9	≥6.7	ns
t_{RLDX}	read enable low to data transition	=1	=2	=1.3	=1.6	ns
t_{RLDV}	read enable low to data valid	=3.5	=7	=4.7	=5.1	ns
t_{DVWL}	data valid to write enable low	≥1.5	≥3	≥0.4	≥0.5	ns
t_{WLDX}	write enable low to data transition	≥1.5	≥3	≥1.5	≥1.6	ns
t_{AVWL}	address valid to write enable low	≥1.5	≥3	≥2.7	≥3.0	ns
t_{WLAX}	write enable low to address transition	≥4.5	≥9	≥2.7	≥3.0	ns
t_{WHWL}	write enable high to write enable low	≥4	≥7	≥2.8	≥3.2	ns
t_{WLWH}	write enable low to write enable high	≥8	≥16	≥ x <5		ns

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OTIS CONTROL ALGORITHM

- Implementation of control elements in Verilog exists
- Simulation of:
  - Verilog Code exists
  - FPGA Code exists
- Tests on FPGA are running

  The FPGA is used for verification of the OTIS CONTROL ALGORITHM.

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Implemented Elements

- Bunch crossing Counter
- Pipeline Control
- Copy to Derandomizing Buffer
- Derandomizing Buffer Control
- Readout Control
  - 1, 2, 3 Bunch crossings per Trigger
  - Optional Bunch crossing Reuse
- Trigger Counter

Simulation and Synthesis for FPGA and ASIC

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Summary

- OTISDLL1.0
  - Lock Range — 30...50 Mhz
  - Clock, Hit Signals — differential
  - DNL — 0.79 Bins @40MHz
  - Problems:
    cross talk from MUX — Guard Ring cut needed
- MEMORY
  - Functional Test — successful
  - Timing — within specification
- CONTROL ALGORITHM
  - Logic synthesizable for FPGA and ASIC
  - Tests on FPGA are in progress

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Next steps

- DLL:
  - Simultaneous operation of MEMORY and DLL
    (Power consumption, cross talk → DNL etc.)
  - Guard-Ring cut to reduce noise from MUX
- Derandomizing Buffer:
  - Timing (Beetle SR Test chip)
- CONTROL ALGORITHM:
  - Ongoing tests with FPGA
  - Design for Test:
    Memory Self test
    Implementation of external memory access
- Fast serial link via GOL-chip

Future Steps

- Specification until October 2001
- Submission of first complete OTIS prototype in February 2002